SECTION III

CIRCUIT DESCRIPTION

3.1 GENERAL

This section describes the various circuits of the WJ-8718 Series HF Receiver. A brief overall description of the four functional sections of the receiver is followed by a module level functional description. An overall functional block diagram is included to show functional signal flow through the receiver. The receiver functional description is followed by detailed circuit-level descriptions of each receiver module. The circuit descriptions are arranged in numerical order to facilitate ease of location.

The WJ-8718 Series Receiver, shown in **Figure 3-1**, is a triple-conversation, superheterodyne receiver which operates in the frequency range from 5 kHz to 30 MHz. It has selected bandwidths between 0.3 kHz and 16 kHz and demodulators for AM, FM, CW, ISB, LSB and USB. Tuning is in discrete 10 Hz steps, locked by frequency synthesizers to an internal or external frequency standard for accuracy and stability. The power supply section provides regulated voltages of ±15 V, +12 V (WJ-8718A/8718-9 only), and +5 V.

3.2 OVERALL RECEIVER DESCRIPTION

The receiver is divided into four functional sections: receiver, synthesizer, digital control and power supply. Refer to **Figure 3-1**, Receiver Overall Block Diagram, as an aid in understanding the Overall Receiver Description.

3.2.1 RECEIVER SECTION

Signals enter the receiver via the RF input connector on the rear panel. The RF Filter (A2) limits the input frequencies to a range of 5 kHz to 30 MHz. These signals are passed to the Input Converter (A3) where the receiver tuned frequency band is mixed with the 1st and 2nd LO signals and converted to the 10.7 MHz 2nd IF. The IF bandwidth at this point is fixed at 16 kHz by the Input Converter. The 10.7 MHz IF is applied to the IF section (A4) where it is mixed with the 3rd LO and converted to the 3rd IF, 455 kHz. The IF bandwidth within A4 is selectable from the front panel. In the AM, FM or CW modes, the IF bandwidth is selected from 0.3, 1.0, 3.2, 6 or 16 kHz. In the USB, LSB and ISB modes, the 455 kHz IF is automatically fixed at 2.95 kHz. The 455 kHz IF is demodulated in the AM, FM, CW, USB, LSB or ISB detection mode as selected via the front panel. Audio from the selected mode is applied through output transformer T2 which is applied to the LINE AUDIO output connector on the rear panel. In the ISB detection mode, the detected USB audio is applied to the LINE AUDIO output while the detected LSB audio is applied to the ISB AUDIO output connector on the rear panel. The output from the FM/CW/SSB detector is applied to the rear panel FM MONITOR terminal. The 455 kHz IF is applied to the rear panel IF OUTPUT jack. Receiver gain is controlled from the front panel and is selected from manual, AGC Fast or AGC Slow. In manual mode, the RF Gain knob on the front panel controls the gain.

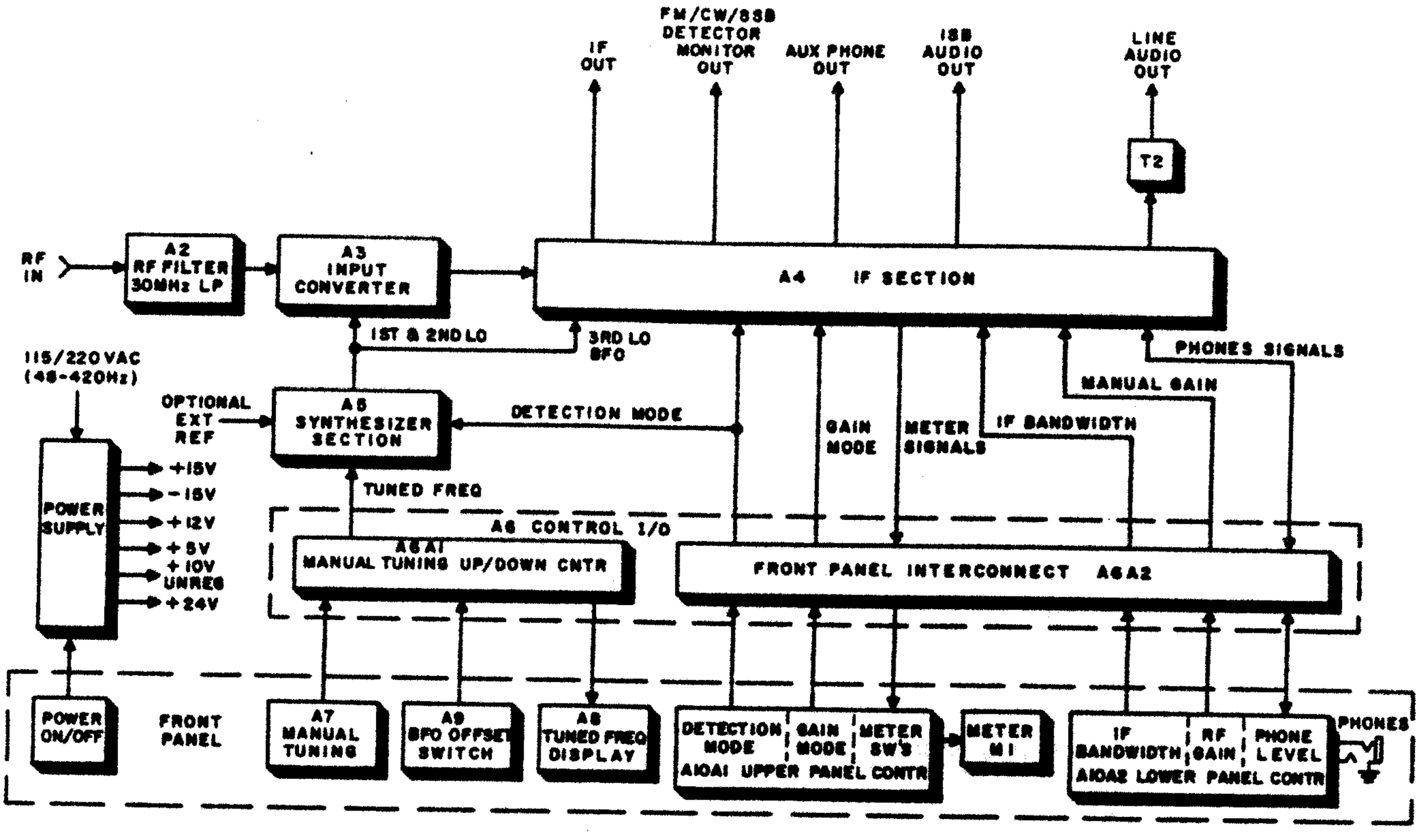


Figure 3-1. Receiver Overall Block Diagram.

3.2.2 SYNTHESIZER SECTION

The Synthesizer Section (A5) contains the 1st, 2nd, 3rd and BFO Synthesizers. A stable Time Base locks the four synthesizers to their respective operating frequencies. The 1st, 2nd and 3rd LO signals are used by the Receiver Section to convert the receiver tuned frequency to 455 kHz. The specific operating frequencies of the 1st and 2nd LO's are programmed by incremental tuned frequency BCD data from the Digital Control Section. The 3rd LO is locked to a fixed frequency of 11.155 MHz. When operating in a CW or SSB mode, the BFO beats with the 455 kHz IF to produce an audio output. The time base is derived from an internal crystal oscillator or an external reference source.

3.2.3 DIGITAL CONTROL SECTION

3.2.3.1 Receiver Tuning Control

Receiver tuning parameters are controlled from the front panel through the Manual Tuning Up/Down Counter (A6A1) and the Front Panel Interconnect (A6A2) on the I/O Motherboard (A6). The Manual Tuning Up/Down Counter contains the RF frequency data. This information is sent to the Synthesizer Section and is also encoded for multiplexing to the

Frequency Display. Frequency data is changed by the Manual Tuning (A7) on the front panel. The Manual Tuning is connected to the Manual Tuning Up/Down Counter and controls the direction and rate of change of the tuned frequency.

The Frequency Display (A8) accepts the multiplexed information from the Up/Down Counter and displays it on the seven LED's of the front panel located display.

The BFO Switch (A9) provides a variation of 0.0 ±08.9 kHz from 455 kHz. It gives a direction of offset and a selectable amount. A zero setting in the directional control automatically returns the BFO to 455 kHz.

3.2.3.2 Front Panel Control

The Front Panel Controls (A10A1) and A10A2) allow manual selection of detection mode, gain mode, meter mode, IF bandwidth, RF gain, and headphone levels. For all detection modes except ISB, the front panel phones jack will yield the Line Audio output. In the ISB detection mode, phones jack audio is selectable between USB and LSB in the WJ-8718A/8718-9, and provides USB and LSB simultaneously in the WJ-8718. The front panel Phone Level control sets the output level. The phone output is sent back through an amplifier in the IF section and is applied to the rear panel as the Aux. Phone output.

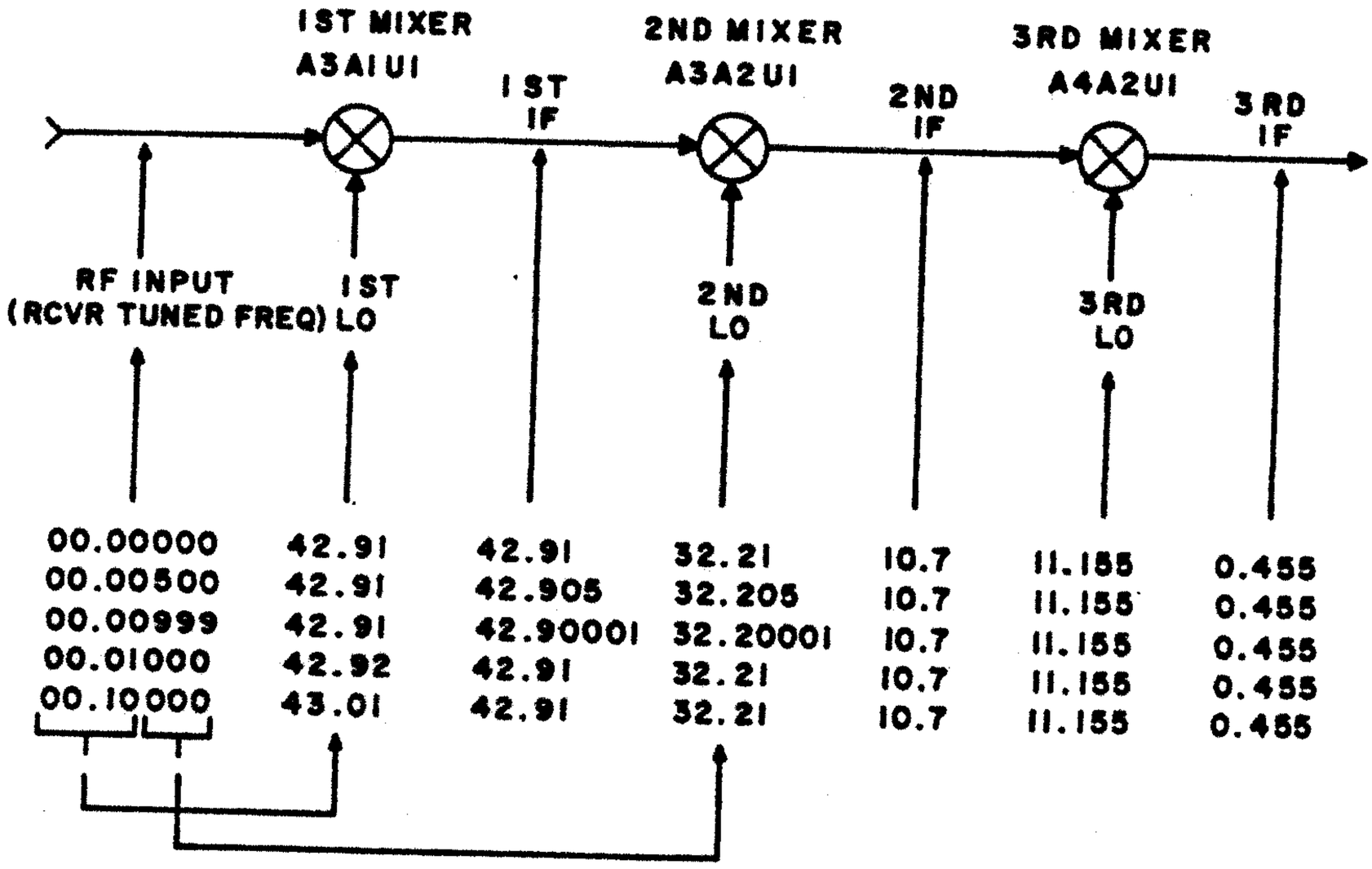
3.2.4 POWER SUPPLY SECTION

The receiver may be operated from either 115 or 230 Vac. The Power Supply Section of the receiver accepts the input voltage via a filter assembly, the input fuses, a voltage selector and the power switch. The input voltage passes to the receiver's transformer which then supplies two lesser ac voltages to the power distribution board. Through the use of rectifiers and voltage regulators, these ac voltages are converted to ±15 V, +12 V (WJ-8718A/8718-9 only), +5 V and unregulated +10 V, which are, in turn, supplied to the various units of the receiver.

3.3. FUNCTIONAL THEORY OF OPERATION

3.3.1 GENERAL

This section describes functional signal flow through the Receiver Section. The signal and control relationships between the Receiver Section and the Synthesizer/Digital Control Sections are explained where necessary to understand receiver functional signal flow. Power Supply Section Functional Operation and Distribution will be discussed separately in **Paragraph 3.3.6.** Refer to **Figure 3-2,** Receiver Functional Block Diagram and **Figure 3-3,** Receiver Frequency Conversion as an aid in understanding Receiver Functional Operation.



NOTE: ALL FREQ'S IN MHz

Figure 3-3. Receiver Frequency Conversion.

3.3.2 INPUT CONVERSION

3.3.2.1 Type 791616-1 RF Filter (A2)

The RF Filter (A2) is a 15-pole low pass filter with a 50 Ω characteristic impedance and a 3 dB nominal loss. RF input signal are band-limited to 5 kHz to 30 MHz by the RF Filter and are applied to the Input Converter (A3).

3.3.2.2 Type 791592-1 Input Converter (A3)

The 1st Mixer receives RF Input signals from the RF Filter (A1) and an LO Signal from the 1st LO Synthesizer (A5A1). The 1st LO is programmed from the four MSDs of receiver tuned frequency and produces a 1st LO frequency of 42.91 to 72.90 MHz. The 1st LO and RF Input signals are mixed by the 1st mixer to produce a first IF in the range of 42.90001 to 42.910 MHz (see **Figure 3-3** for the relationship between RF Input, 1st LO and 1st IF frequencies). The 1st IF signal is amplified and filtered by a 28 kHz bandwidth band-pass filter with a center frequency of 42.905 MHz.

The 2nd Mixer receives the 1st IF signal from the 1st Mixer and an LO signal from the 2nd LO Synthesizer (A5A2). The 2nd LO is programmed by the three LSDs of receiver tuned frequency and produces a 2nd LO frequency of 32.21 to 32.20001 MHz. The 2nd LO and 1st IF are mixed by the 2nd Mixer to produce a 2nd IF of 10.70 MHz (see **Figure 3-3** for the relationship between 1st IF, 2nd LO and 2nd IF frequencies). The 2nd IF signal is amplified and filtered by a 16 kHz bandwidth band-pass filter with a 10.7 MHz center frequency and drives the 50 Ω input of the 10.7 MHz Filter Switch, A4A1.

3.3.3 TYPE 791569-1 IF MOTHERBOARD (A4)

The IF Section, mounted on Motherboard A4 consists of the 3rd Mixer, four IF Filter Switches, three detector boards, an audio amplifier and AGC circuit (see **Figure 3-2**). IF Section functional signal flow will be correlated with control data from the Front Panel. Signal flow will be traced through each of the IF Section modules in a functional rather than numerical sequence.

3.3.3.1 Type 791594-1 10.7 MHz Filter Switch (A4A1)

The 2nd IF output from A3 drives the 50 Ω input of the 10.7 MHz Filter Switch, A4A1-13. The signal is routed through one of three voltage-selectable circuit paths within A4A1. The wideband path, selected by +5 Vdc at pin 15, passes the full 16 kHz bandwidth from A3 through A4A1. The other two circuit paths, selected by +5 Vdc at pin 17 or 19, restricts the bandpass to 6 or 3.2 kHz respectively (see **paragraph 3.3.3.9** for complete explanation of bandwidth selection). The amplified, band-limited output at A4A1-57 drives the 50 Ω input of the 3rd Mixer, A4A2-57.

3.3.3.2 Type 71430-1 10.7 MHz/455 kHz Converter (A4A2)

The amplified 2nd IF output from A4A1-57 drives the 50 Ω input of the 10.7 MHz/455 kHz Converter, or the 3rd Mixer A4A2-57. The 3rd Mixer also receives an LO signal from the 3rd LO Synthesizer, A5A1, which is fixed at a frequency of 11.155 MHz. The 3rd LO and 2nd IF are mixed by the 3rd Mixer to produce a 3rd IF of 455 kHz (see **Figure 3-3** for the relationship between the 2nd IF, 3rd LO and 3rd IF frequencies). The 3rd IF output, A4A2-19, of the 3rd Mixer is stepped up to an impedance of 1000 Ω and drives the parallel-connected inputs of the 455 kHz Filter Switch, A4A3, the USB Filter Switch, A4A4 and the LSB/ISB Filter Switch, A4A5.

3.3.3.3 3rd IF Bandwidth Filtering

The 3rd IF output from the 3rd Mixer passes through one of five IF filters prior to final IF amplification and detection. If the AM, FM or CW Mode has been selected, the 3rd IF will pass through the 455 kHz Filter Switch, A4A3. If a sideband mode has been selected, the 3rd IF will pass through the USB Filter Switch, A4A4 or the LSB/ISB Filter Switch, A4A5.

3.3.3.3.1 Type 791595-1 455 kHz Filter Switch (A4A3)

The 3rd IF output from A4A2-19 drives the high-impedance input of the 455 kHz Filter Switch, A4A3-13. When AM, FM or CW Mode is selected, the signal is routed through one of three voltage-selectable circuit paths within A4A3. The wideband path, selected by +5 Vdc of pin 15, passes the full bandwidth, determined by A3 and A4A1, through A4A3. The other two circuit paths, selected by +5 Vdc at pin 17 or 19, narrow the bandpass from that determined by A3 and A4A1 down to 1.0 kHz or 0.3 kHz respectively (see **paragraph 3.3.3.9** for complete explanation of bandwidth selection). The amplified, band-limited output from A4A3-57 drives the high-impedance input of the 455 kHz IF Amplifier/Demodulator, A4A7-57.

3.3.3.3.2 Type 791596-1 USB Filter Switch (A4A4)

The 3rd IF output from A4A2-19 drives the high-impedance input of the 455 kHz Filter Switch, A4A3-13. In USB Mode, selected by +5 Vdc at pin 49, or in ISB Mode, selected by +5 Vdc at pin 51, the IF signal passes through the USB IF Filter within A4A4 (see **Paragraph 3.3.3.10** for complete explanation of mode selection). This filter restricts the IF bandwidth to 2.95 kHz (455.25 kHz to 458.2 kHz). The amplified USB IF output at A4A4-57 drives the high-impedance input of the 455 kHz IF Ampl./Demodulator, A4A7-57.

3.3.3.3.3 Type 791597-1 LSB/ISB Fiter Switch (A4A5)

The 3rd IF output from A4A2-19 drives the high-impedance input of the LSB/ISB Filter Switch, A4A5-13. In LSB Mode, selected by +5 Vdc at pin 49, or in ISB Mode, selected by +5 Vdc at pin 51, the IF signal passes through the LSB IF filter within A4A5 (see **paragraph 3.3.3.10** for complete explanation of mode selection). This filter restricts the bandwidth to 2.95 kHz (451.8 kHz to 454.75 kHz). In LSB Mode, the amplified LSB IF output at A4A5-57 drives the high-impedance input of the 455 kHz IF Ampl/Demodulator, A4A7-57. In ISB Mode, the amplified LSB IF output at A4A5-53 drives the high impedance input of the ISB Detector/ Audio, A4A8-53.

3.3.3.4 Type 72488-1 455 kHz Ampl/AM Detector (A4A7)

The amplified 3rd IF output from A4A3-57, A4A4-57 or A4A5-57 drives the high impedance input of the 455 kHz IF Ampl/Detector, A4A7-57. The signal is amplified by a two-stage gain-controlled (for AGC purposes) amplifier with an overall bandwidth of 30 kHz. Following this, the IF signal is split to provide three outputs: the input to the AM Detector, the third IF output at A4A7-13 which drives the input to the FM/CW/SSB Detector and the 3rd IF ouptut at A4A7-17 which drives the rear panel IF Output jack J2. The AM Audio output from the AM Detector at A4A7-51 contains a DC level proportional to RF Input signal strength and audio resulting from modulation detection by the AM Detector. This AM Audio output drives the parallel-connected inputs of the AGC, A4A6-51, and the Audio Amplifier, A4A10-51.

3.3.3.5 Type 791599-1 FM/CW/SSB Detector (A4A9)

The amplified 3rd IF output from A4A7-13 drives the high-impedance input of the FM/CW/SSB Detector, A4A9-13. In the FM Mode, selected by +5 Vdc at pin 41 (see **Paragraph 3.3.3.10**), the signal is amplified, limited and drives an FM discriminator. The audio from the discriminator is amplified by a summing amplifier and appears as FM Audio at A4A9-57. In the CW or any of the sideband modes, selected by +5 Vdc at pin 43 (see **Paragraph 3.3.3.10**), the signal is applied to a product detector. The BFO Synthesizer is also enabled and supplies a fixed (SSB mode) or variable (CW mode) 455 kHz BFO signal to A4A9-17. This BFO signal mixes with the 3rd IF signal in the product detector. The audio from the product detector is amplified by the summing amplifier, and appears as CW/SSB Audio at A4A9-57. Audio from A4A9-57 drives the input of the Audio Amplifier, A4A10-57 and also appears on the rear panel TB2 as FM AUDIO.

3.3.3.6 Type 746001-1 Audio Amplifier (A4A10)

The AM Audio output from A4A7-57 drives the input to the Audio Amplifier, A4A10-57, and the FM/CW/SSB Audio output from A4A9-51 drives the input to the Audio Amplifier, A4A10-51. In AM mode, selected by +5 Vdc at pin 47 (see **Paragraph 3.3.3.10**), the AM Audio at pin 57 is gated through a summing amplifier at unity gain and appears at pin 55. In FM, CW or SSB Modes, pin 47 is 0 Vdc, and the FM/CW/SSB Audio at pin 51 is gated through the summing amplifier and appears at pin 55. Combined Audio at pin 55 has two destinations: the Headphone Amplifier in A10-A2 and the rear panel Line Audio Level control. The function of the headphone amplifier will be explained in **Paragraph 3.3.5.6.2**. The Line Audio Level control attenuates the audio signal from pin 55 and applies it to the Audio Amplifier via pin 17. A push-pull Line Audio amplifier amplifies the signal and outputs it at A4A10-11, 13. Transformer T2 on the rear panel matches to low impedance output at pins 11 and 13 to a 600 Ω line. The high level Line Audio signal appears on rear panel TB1. A rectifier samples the output of the A4A10 Line Audio amplifier and supplies the front panel meter in the LINE AUDIO setting. A low level audio signal from the A4A10-53 and drives the Auxiliary Phone amplifier. The Auxiliary Phone out signal at A4A10-19 appears at the rear panel TB1, PHONE AUDIO.

3.3.3.7 Type 791598-1 ISB Detector/Audio (A4A8) (Optional in WJ-8718/8718-9)

The amplified LSB IF signal from A4A5-53 drives the high impedance input of the ISB Detector/Audio, A4A8-53. In the ISB Mode, selected by +5 Vdc at pin 49 (see **Paragraph 3.3.3.10**), the LSB IF signal is amplified by two tuned stages and applied to a product

detector. The BFO signal mixes with the LSB IF signal in the product detector. The audio from the product detector appears at A4A8-41 as ISB Audio and goes through the Mode Switch to the Headphone Amplifier in A10A2 (see **Paragraph 3.3.5.6.2**). The ISB Audio from the product detector is also amplified by a push-pull amplifier stage. This provides a high level balanced ISB Line Audio terminals on rear panel TB1. An AGC circuit within A4A8 samples the ISB Audio from the product detector and adjusts the gain of the two-stage tuned amplifier that feeds the product detector. A sample of the AGC voltage appears at A4A8-43 and is applied to the main AGC module, A4A6-43, to produce a combined RF AGC.

3.3.3.8 Type 78112-1 AGC (A4A6)

The AM Audio output from A4A7-51 drives the input of the AGC, A4A6-51. In AGC mode, selected by 0 Vdc at pin 13, a filter network removes the audio modulation and the resulting DC level is amplified and output as the IF GC Voltage at A4A6-47. This voltage adjusts the gain of the IF Amplifier, A4A7. Under very strong input signal conditions, a gate circuit transfers the IF GC voltage to pin 19, RF GC, permitting a reduction in Input Converter gain. The ISB AGC signal, entering through pin 43, is summed through this gate to permit the ISB AGC to reduce the Input Converter Gain. A4A6-41, AGC Signal Strength, is a DC sample of the IF GC voltage that drives the front panel meter in Signal Strength Mode. In the MAN gain mode, selected by +5 Vdc at pin 13, the IF and RF GC outputs respond to the MAN GAIN, A4A6-17, signal from the front panel RF GAIN control. A4A6-12, MAN Signal Strength, is a DC sample of the AM Audio, A4A6-51, signal that drives the front panel meter in the Signal Strength Mode.

3.3.3.9 Bandwidth Selection

Bandwidth selection is accomplished via voltage-selectable filters in the 2nd and 3rd IF amplifiers. The select voltages are TTL compatible (0 Vdc = OFF, +5 Vdc = ON). In AM, FM and CW modes, the Front Panel Bandwidth switches are energized. Selection of a particular bandwidth sends +5 Vdc from A10A2S1 to the appropriate filters in A4A1 and A4A3. In USB, LSB or ISB Modes, the Front Panel Bandwidth switches are disabled. A4A1 is fixed in the wide position, and A4A4 or A4A5 is selected, as required. **Table 3-1** summarizes the relationship between Detector Mode, Bandwidth and filter selection.

3.3.3.10 Mode Selection

Mode selection is accomplished via TTL-compatible (0 Vdc = OFF, +5 Vdc = ON) select voltages from the Front Panel Detection Mode switches. Selection of a particular mode sends +5 Vdc from A10A1S3 to the appropriate IF section modules. As discussed in **Paragraph 3.3.3.9**, the mode switches also determine the 2nd and 3rd IF bandwidth in SSB Modes. The output of the AM detector, A4A7-51, is active on all modes since it is used to develop AGC voltages in A4A6. **Table 3-2** summarizes the Detection Mode selection relationships.

3.3.4 TYPE 791570-1 SYNTHESIZER SECTION (A5)

The Synthesizer Section, shown in **Figure 3-2**, consist of the 1st, 2nd, 3rd and BFO Synthesizers and the Time Base. The synthesizers receive digital commands from the

Man. Tuning Up/Down Counter and set the L O signals to the correct frequencies as dictated by the receiver tuned frequency. The relation between receiver tuned frequency and L O frequency is shown in **Figure 3-3.**

Table 3-1. 2nd and 3rd IF Bandwidth Selection

BW Filter Select Pin	BW Switch Selection (AM, FM, CW Mode) 16	6	3.2	1.0	0.3	SSB Modes USB	LSB	ISB
A4A1-15 (W1)	+5	0	0	0	0	+5	+5	+5
A4A1-17 (6 kHz)	0	+5	0	0	0	0	0	0
A4A1-19 (3.2 kHz)	0	0	+5	+5	+5	0	0	0
A4A3-15 (W2)	+5	+5	+5	0	0	0	0	0
A4A3-17 (1.0 kHz)	0	0	0	+5	0	0	0	0
A4A3-19 (0.3 kHz)	0	0	0	0	+5	0	0	0
A4A4-49 (USB)	0	0	0	0	0	+5	0	0
A4A4-51 (ISB)	0	0	0	0	0	0	0	+5
A4A5-49 (LSB)	0	0	0	0	0	0	+5	0
A4A5-51 (ISB)	0	0	0	0	0	0	0	+5

Table 3-2. Detection Mode Selection.

Mode Select Pin	Detection Mode Switch Selection AM	FM	CW	USB	LSB	ISB
A4A10-47(AM SEL)	+5	0	0	0	0	0
A4A9-41 (FM)	0	+5	0	0	0	0
A4A9-43 (CW/SSB)	0	0	+5	+5	+5	+5
A4A8-49 (ISB)	0	0	0	0	0	+5
A5A3-43 (OFFSET EN.)	0	0	+5	0	0	0
A5A3-57 (BFO INH)	+5	+5	0	0	0	0

3.3.4.1 Type 791630-1 1st L.O. Synthesizer (A5A1)

The 1st LO receives BCD tuned frequency command data from the four MSDs of the receiver tuned frequency readout. The BCD numbers range in value of 0000 to 2999 corresponding to receiver tuned frequencies of 00.00XXX MHz to 29.99XXX MHz. The output of the 1st LO tunes from 42.91 MHz to 72.90 MHz in 10 kHz steps in accordance with the BCD tuned frequency data. A stable 40 kHz time base signal provides a precise reference for the 1st LO phase lock loop control circuits.

3.3.4.2 Type 791601 2nd L.O. Synthesizer (A5A2)

The 2nd LO receives BCD tuned frequency command data from the three LSD's of the receiver tuned frequency readout. The BCD numbers range in value from 000 to 999 corresponding to receiver tuned frequencies of XX.XX000 MHz to XX.XX999 MHz. The output of the 2nd LO tunes down from 32.21000 MHz to 32.20001 MHz as the BCD data increments from 000 to 999. Stable 10 kHz and 1 MHz time base signals provide precise references for the 2nd LO phase lock loop control circuits.

3.3.4.3 3rd L.O. Synthesizer (P/O A5A1)

The 3rd LO Synthesizer produces a fixed frequency output of 11.155 MHz. Basic frequency control is obtained by an 11.155 MHz crystal oscillator. The exact frequency of oscillation is precisely locked to 10 kHz and 50 kHz time base reference signals by a phase locked loop.

3.3.4.4 Type 791576-1 BFO Synthesizer (A5A3)

The BFO Synthesizer receives BCD offset frequency command data from the MSD and LSD of the BFO offset switch, A9. The BCD numbers range in value from 00 to 89 corresponding to offset frequencies of 0.0 kHz to 8.9 kHz. Offset control data from the "+, 0, -" switch section of A9 programs the direction of BFO offset. The output of the BFO tunes from 446.1 kHz (455 kHz - 8.9 kHz) to 463.9 kHz (455 kHz + 8.9 kHz). In the AM and FM modes, BFO INH, A4A8-57, is high, shutting off the BFO output at A5-P15, even though the BFO itself is oscillating. In SSB modes, OFFSET ENABLE, A4A8-43 is low, fixing the BFO output at 455.000 kHz. A stable 1 kHz time base signal provides a precise reference for the BFO phase lock loop control circuits.

3.3.4.5 Time Base (P/O A5A1)

All four synthesizer circuits are synchronized by a common Time Base. Reference frequencies of 1 MHz, 50 kHz, 40 kHz, 10 kHz, and 1 kHz are supplied from a 2 MHz temperature compensated crystal oscillator or from a 1 MHz external source input at rear panel jack J11. The rear panel INT/EXT clock switch S2 allows selection at the internal and external reference. When in the internal mode, the 1 MHz internal reference is output from rear panel jack J11.

3.3.5 DIGITAL CONTROL SECTION

The Digital Control section is composed of the Manual Tuning Up/Down Counter; the Front Panel Interconnect; the Manual Tuning Module; the Frequency Display; the BFO Switch, the Upper Panel Control and the Lower Panel Control. **Figure 3-2** shows the overall relationship of these units.

3.3.5.1 Type 791575-3 Manual Tuning Up/Down Counter (A6A1)

The Manual Tuning Up/Down Counter contains the RF tuned frequency data. This information is sent to the 1st and 2nd LO Synthesizers and is encoded for multiplexing to the display board. The frequency data is changed by means of the Encoder on the Manual Tuning Module on the front panel.

3.3.5.2 Type 791828-1 Front Panel Interconnect (A6A2)

This module translates information received from the manually controlled front panel into control information for the receiver. Front panel information entering this module controls detection mode, gain mode, meter mode, and IF bandwidth, in addition to headphone and RF gain levels. This information is then decoded, for use primarily in the IF stages of the receiver. Two output lines from the Front Panel Interconnect, however, control the BFO for the various detection modes.

3.3.5.3 Type 791874-1 Manual Tuning Module (A7)

The Manual Tuning Module contains the Encoder U1 and Tuning Resolution Switches A7A1. Switching is accomplished by connecting the desired tuning step to the step select switch line of the Manual Tuning Up/Down Counter board. Tuning steps available are 10 Hz, 100 Hz, 1 kHz, and 10 kHz.

3.3.5.4 Type 791578-1 Frequency Display (A8)

The Frequency Display accepts the multiplexed information from the Manual Tuning Up/Down Counter and displays it on the seven front panel LEDs. These are seven-segment common-cathode displays which are controlled by an IC decoder/driver. The Up/Down Counter places digit display information in the IC where it is decoded into the proper number and sent to the display in its proper position.

3.3.5.5 Type 791827 BFO Switch (A9)

Three thumbwheel switches provide a BFO variation of ±8.9 kHz from 455 kHz. The +, 0, -, thumbwheel provides the direction of offset, the second thumbwheel varies in range from 0 to 8, and the third thumbwheel varies in range from 0 to 9. A "0" setting of the direction thumbwheel causes the BFO to return automatically to 455 kHz regardless of the other thumbwheel settings.

3.3.5.6 Type 796053 Front Panel Control (A10)

The Front Panel Control consists of the Upper and Lower Panel Control boards joined by a 40-pin ribbon connector. This connector is attached to the Front Panel Interconnect (A6A2) and controls the manual selection of detection mode, gain mode, meter mode, IF bandwidth, RF gain, and heaphone levels. Signals for the phone outputs also connect to the lower panel control through the Front Panel Interconnect.

3.3.5.6.1 Type 791583 Upper Panel Control (A10A1)

The Upper Panel Control allows selection of detection mode, gain mode, and meter mode. Each gang of switches mechanically operates to allow one pushbutton to be depressed at any time. All control lines connect to the Front Panel Interconnect card.

3.3.5.6.2 Type 796054 Lower Panel Control (A10A2) (WJ-8718A/8718-9)

The Lower Panel Control allows selection of IF bandwidth and variation of RF gain and phone level potentiometers. This card also contains the amplifier to drive the headphone output. The amplifier receives the Line Audio signal in all detection modes except ISB. In this mode, the amplifier switches between the upper sideband and the lower sideband information.

3.3.5.6.3 Type 791826 Lower Panel Control (A10A2) (WJ-8718)

The Lower Panel Control allows selection of IF bandwidth and variation of RF gain and phone level potentiometers. This card also contains the headphone amplifier. The amplifier receives the Line Audio signal in all modes except ISB. In ISB mode, the headphone amplifier simultaneously amplifies the separated upper and lower sideband audio signals.

3.3.6 POWER SUPPLY SECTION

See **Figure 3-4** for the power supply block diagram. The receiver may be operated from either 110 Vac, 120 Vac, 220 Vac or 240 Vac. This voltage feeds Filter Assembly FL1 which contains the input voltage selector. It then passes through fuses F1 and F2 and through the main power switch, S1. From the switch, current is routed through the Voltage Selector and into Transformer T1. The Transformer has a dual primary and center-tapped secondaries and produces outputs of 34 and 16 Vac both of which enter the Power Distribution board, (A1).

3.3.6.1 Type 76240 Power Distribution (A1)

The Power Distribution board receives the 34 and 16 Vac inputs and rectifies these voltages for various circuits in the receiver. The 34 Vac enters this board, is rectified and filtered and sent to regulators U1, U2 and U4. The 16 Vac is rectified by two diodes located on the rear panel and returned to the Distribution board to be filtered and become a +10 V unregulated supply.

3.3.6.2 Power Supply Regulators

U1 and U2 located on the back of the chassis provide regulated +15 Vdc and -15 Vdc, respectively. These two voltages are supplied to most of the circuits in the receiver. The unregulated 10 Vdc, with its unregulated ground, connects to U3, a +5 Vdc regulator. U3 supplies +5 Vdc to the BFO and 2nd LO Synthesizers, the Up/Down counter board, and the Front Panel Interconnect card. The unregulated 10 Vdc also connects through other +5 Vdc regulators to provide this voltage to the 1st and 3rd LO Synthesizers. U4 provides regulated +12 Vdc for the Audio Amplifier (A4A10) in the WJ-8718A/8718-9 receivers.

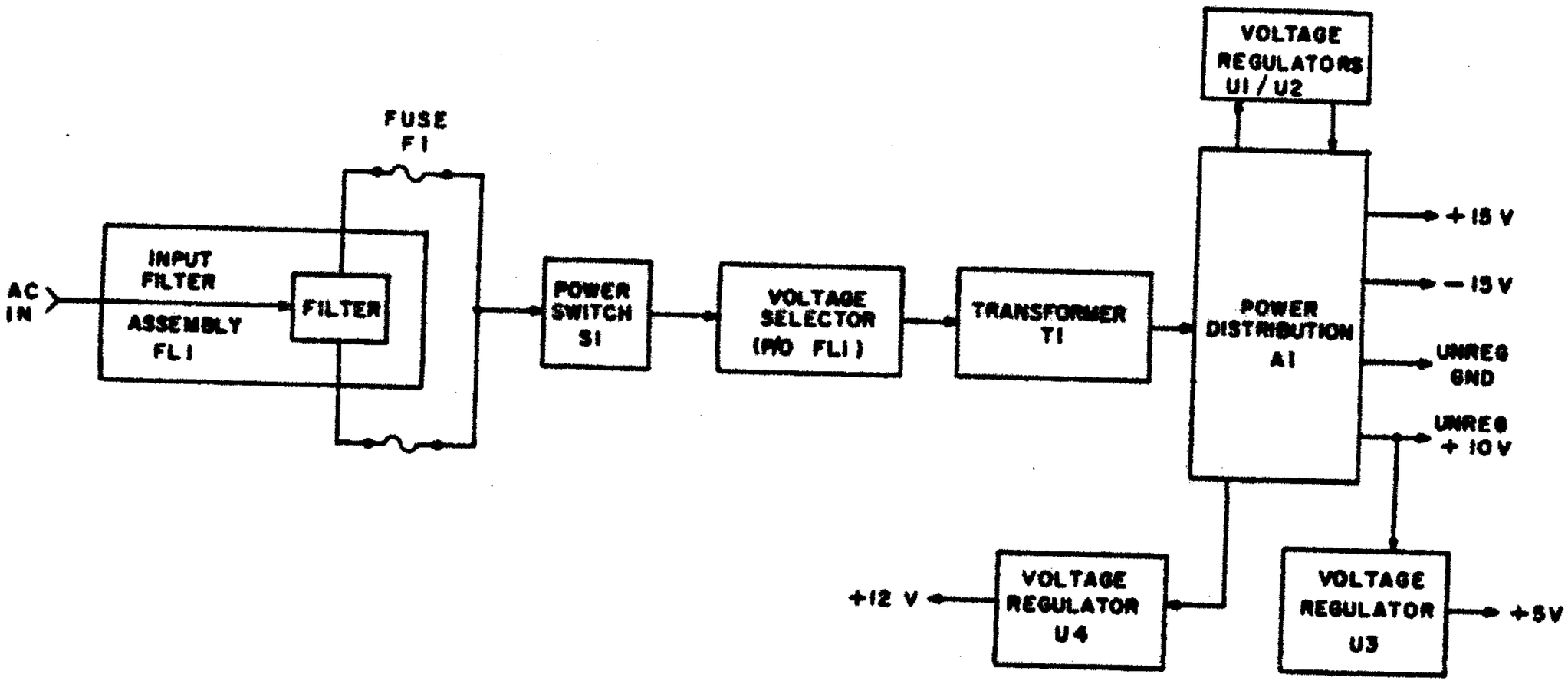


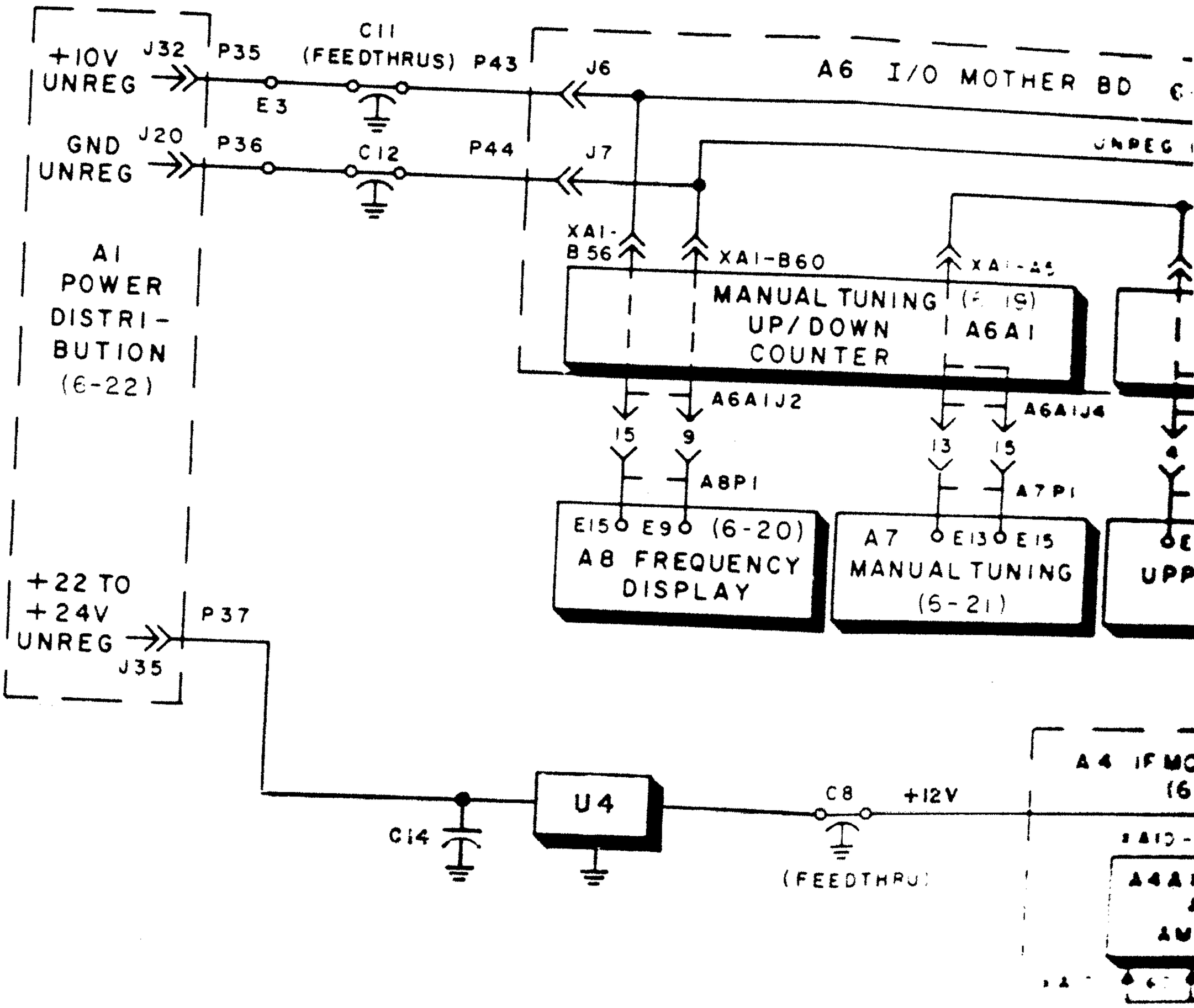
Figure 3-4. Power Supply Section Functional Block Diagram.

3.3.6.3 Power Supply Voltage Distribution

Figure 3-5 is a simplified block diagram showing the interconnections between power supply outputs and main chassis subassemblies and modules.

3.4 CIRCUIT DESCRIPTIONS

This paragraph provides detailed circuit descriptions of the subassemblies and modules contained in the WJ-8718 Series HF Receiver. All significant components are identified and supplementary block diagrams are employed to aid in understanding circuit operation. Modules are discussed in numerical order to facilitate ease of location.


+10V UNREG
J32
P35
E3
C11 (FEEDTHRUS)
P43
J6
A6 I/O MOTHER BD
GND UNREG
J20
P36
C12
P44
J7
XA1-B56
XA1-B60
MANUAL TUNING UP/DOWN COUNTER
A6A1
A6A1J2
A6A1J4
15
9
13
15
A8P1
A7P1
E15
E9
(6-20)
A8 FREQUENCY DISPLAY
A7
E13
E15
MANUAL TUNING
(6-21)
A1 POWER DISTRI-BUTION (6-22)
+22 TO +24V UNREG
J35
P37
C14
U4
C8
+12V
(FEEDTHRU)

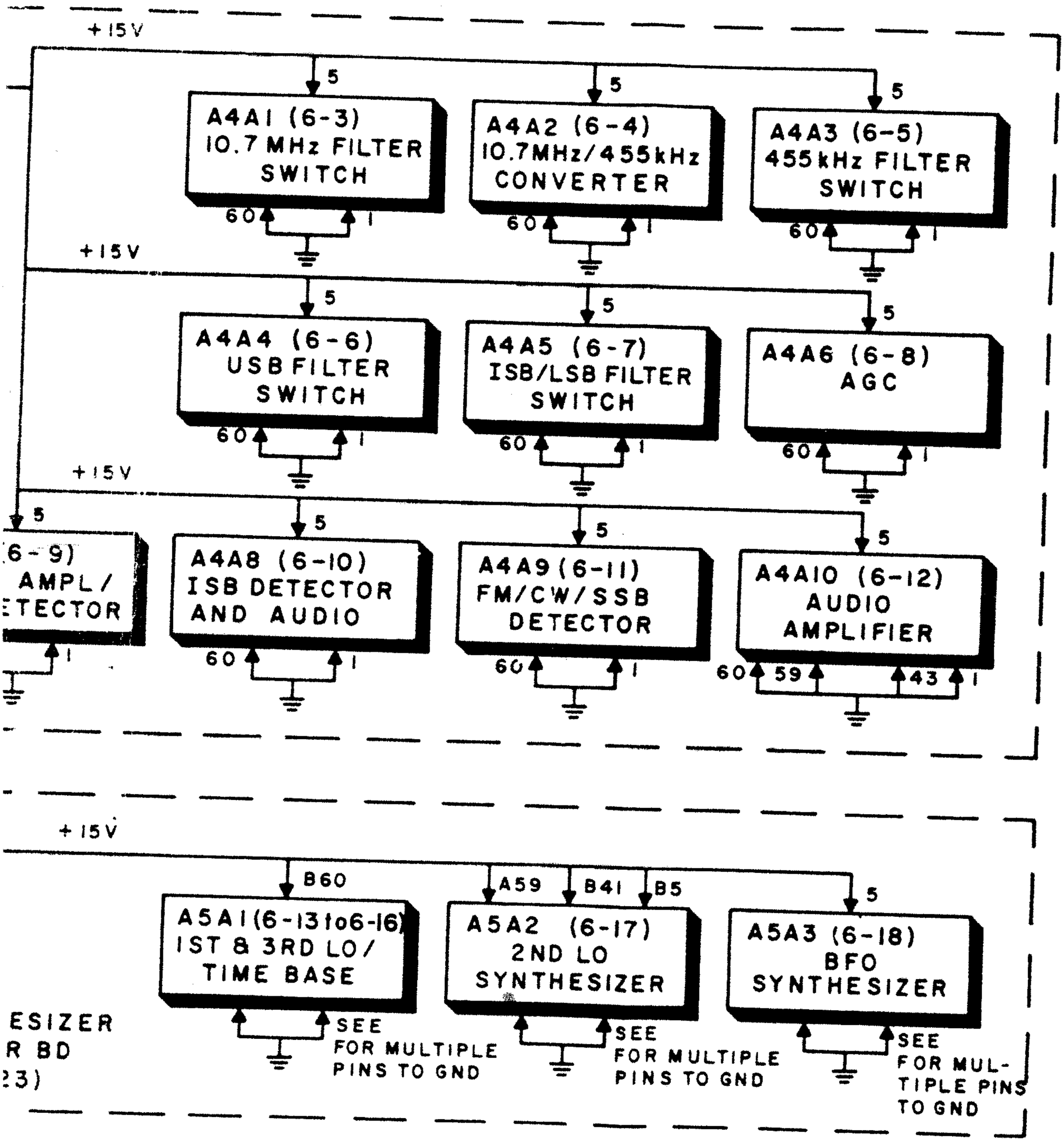


Figure 3-5. Power Supply Voltage Distribution Diagram (Sheet 1 of 3)

POWER SUPPLY
(6-22)
+15V
A1J10
P33
C9
(FEEDTHRU)
E1
P41
J4
J2
3
1
A3P1
C3 (6-2)
A3
INPUT CONVERTER
A6 I/O MOTHER BD
(6-22)
XA2
-57
A6A2 (6-23)
FRONT PANEL
INTERCONNET
A6A2J1
39
A10P1
E2
A10A2
LOWER PANEL CONTROL
(6-21)
A6
J3
28
A4P1
E28
L1
A5P1
1
A6
J1
A4
MOT
BOA
(6-
L2
E1
A5 S
M

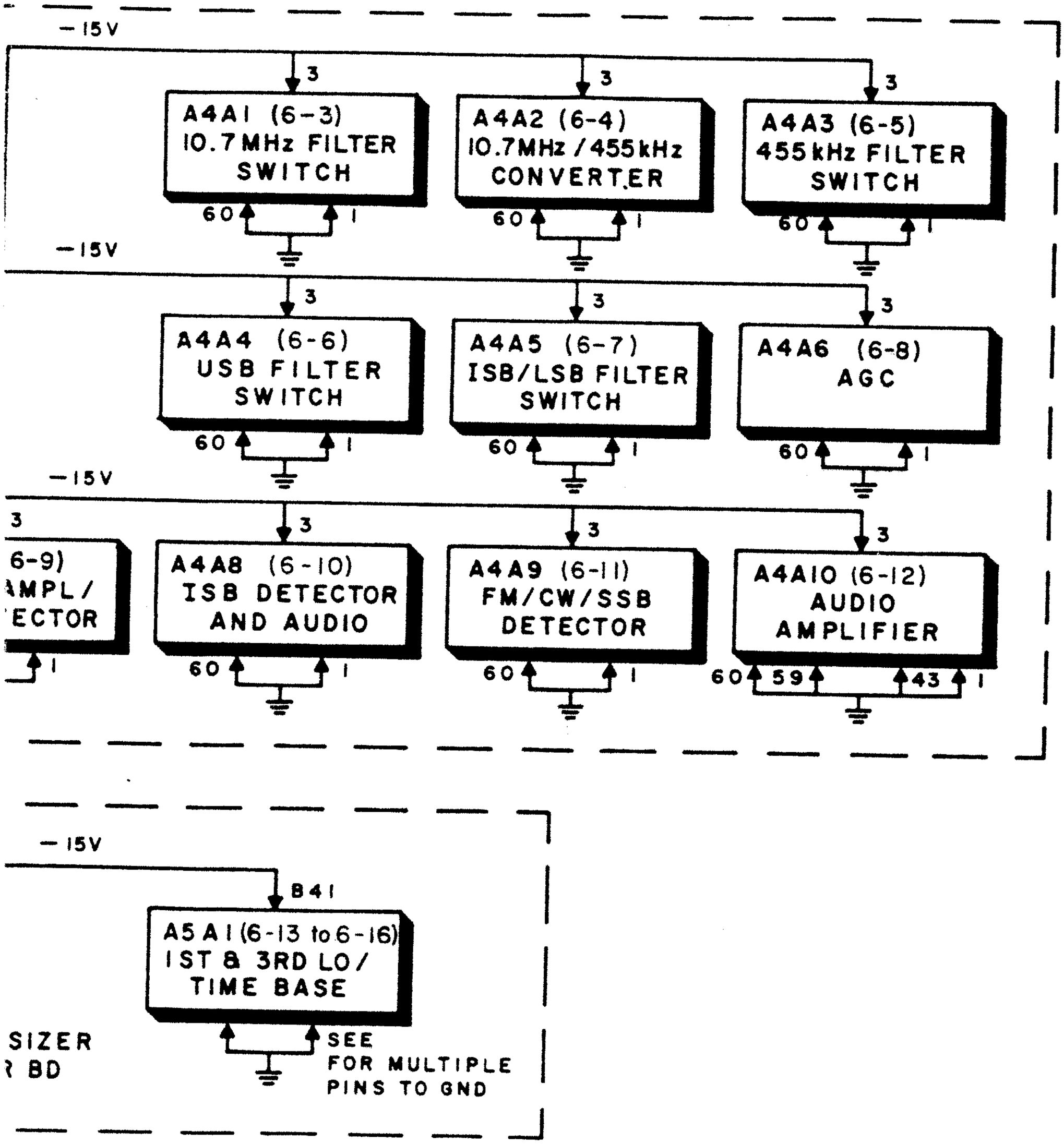


Figure 3-5. Power Supply Voltage Distribution Diagram (Sheet 2 of 3)

POWER SUPPLY
(6-22)
-15V
A1J14
P34
C10
(FEEDTHRU)
E2
P42
J5
J2
3
2
A3P1
A3
INPUT CONVERTER
(6-2)
C2
A6 I/O MOTHER BD
(6-22)
XA2
-59
A6A2 (6-23)
FRONT PANEL
INTERCONNECT
A6A2J1
35
A10P1
E6
A10A2
LOWER PANEL CONTROL
(6-21)
A6
J3
29
A4P1
L2
E29
A5P1
2
A6
J1
A4 IF
MOTHE
BOARD
(6-22)
A4A
455k
AM
60
L3
E2
A5 SYNT
MOT
(6-2

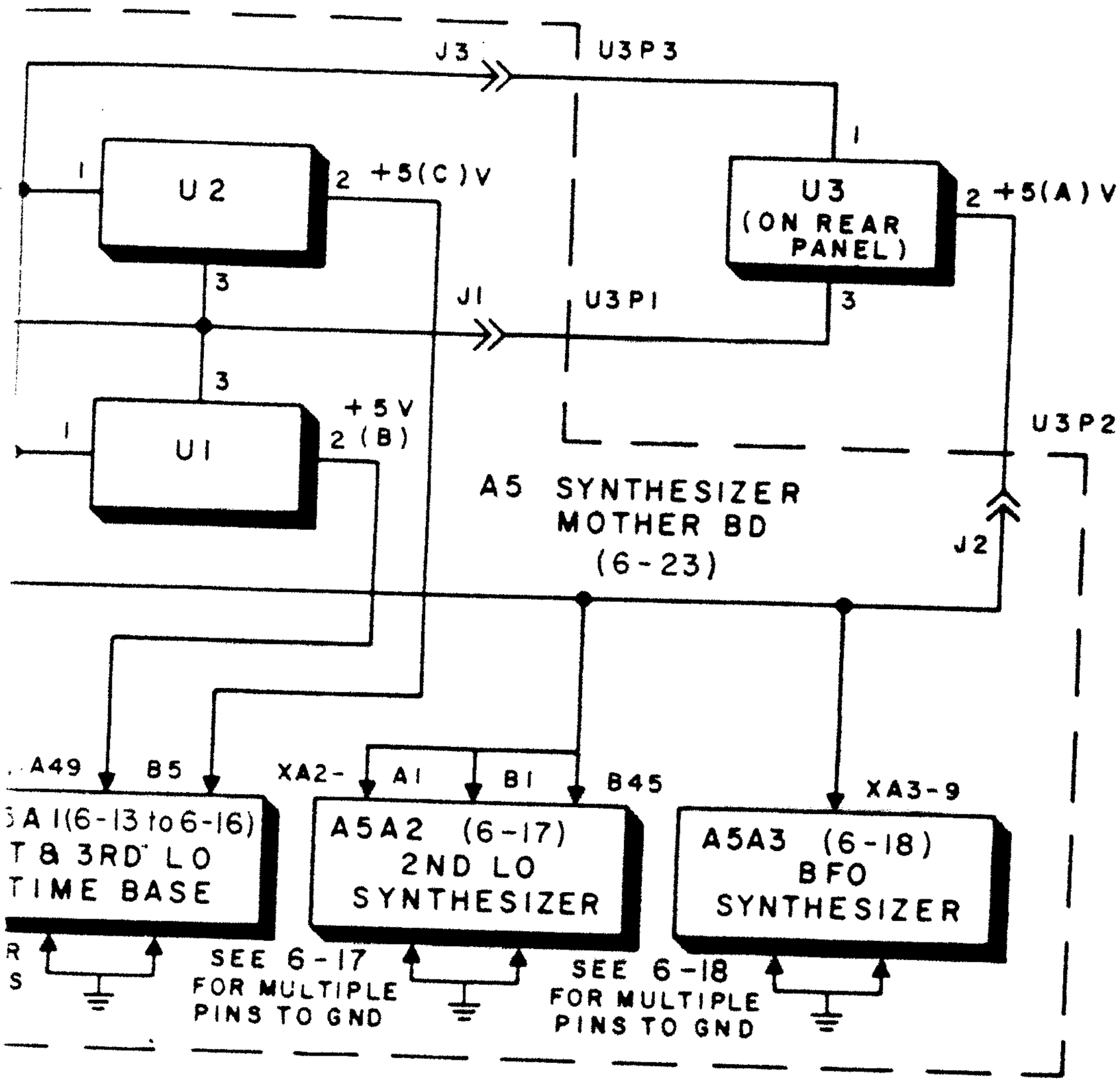


Figure 3-5. Power Supply Voltage Distribution Diagram
(Sheet 3 of 3)

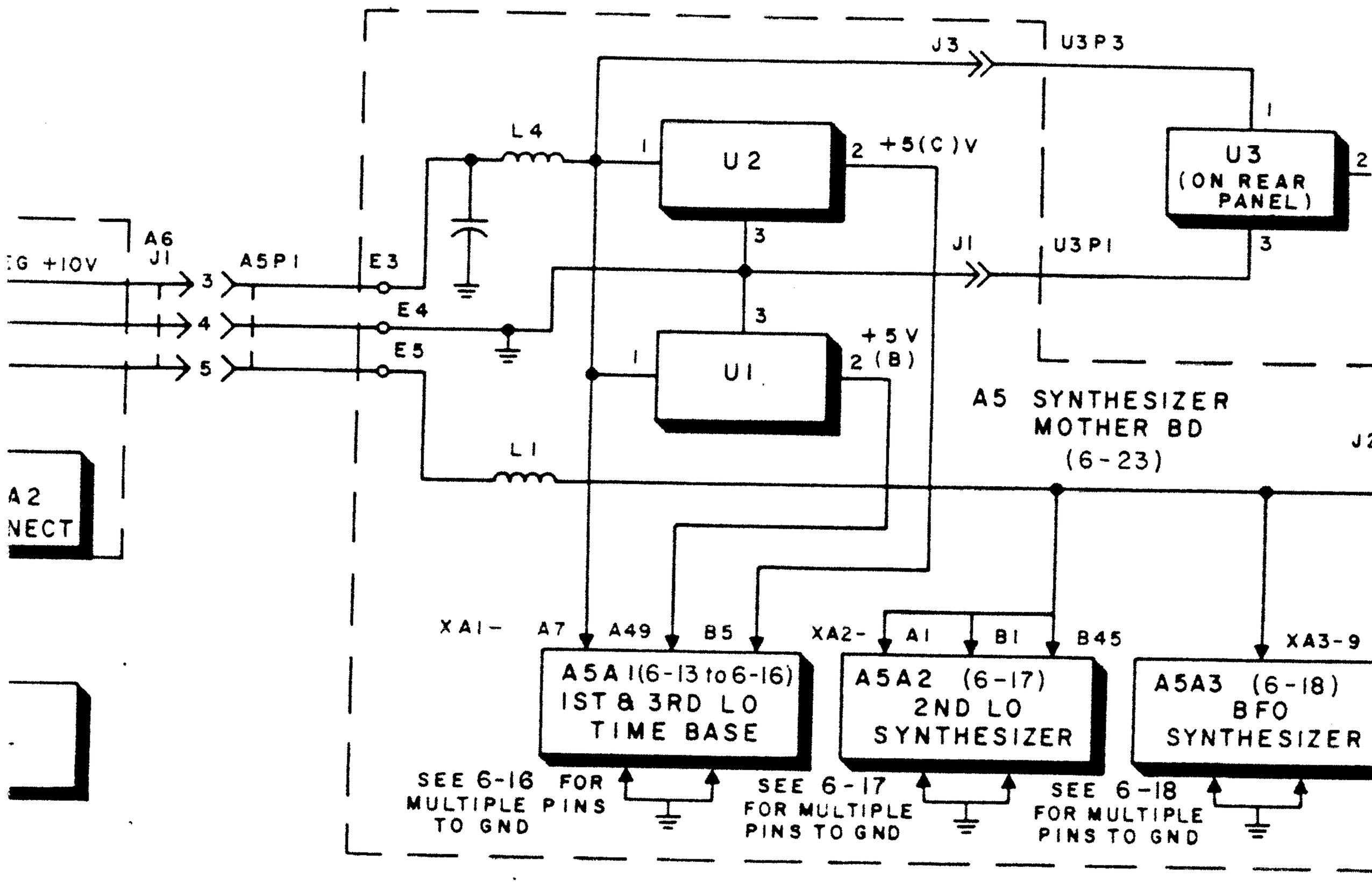
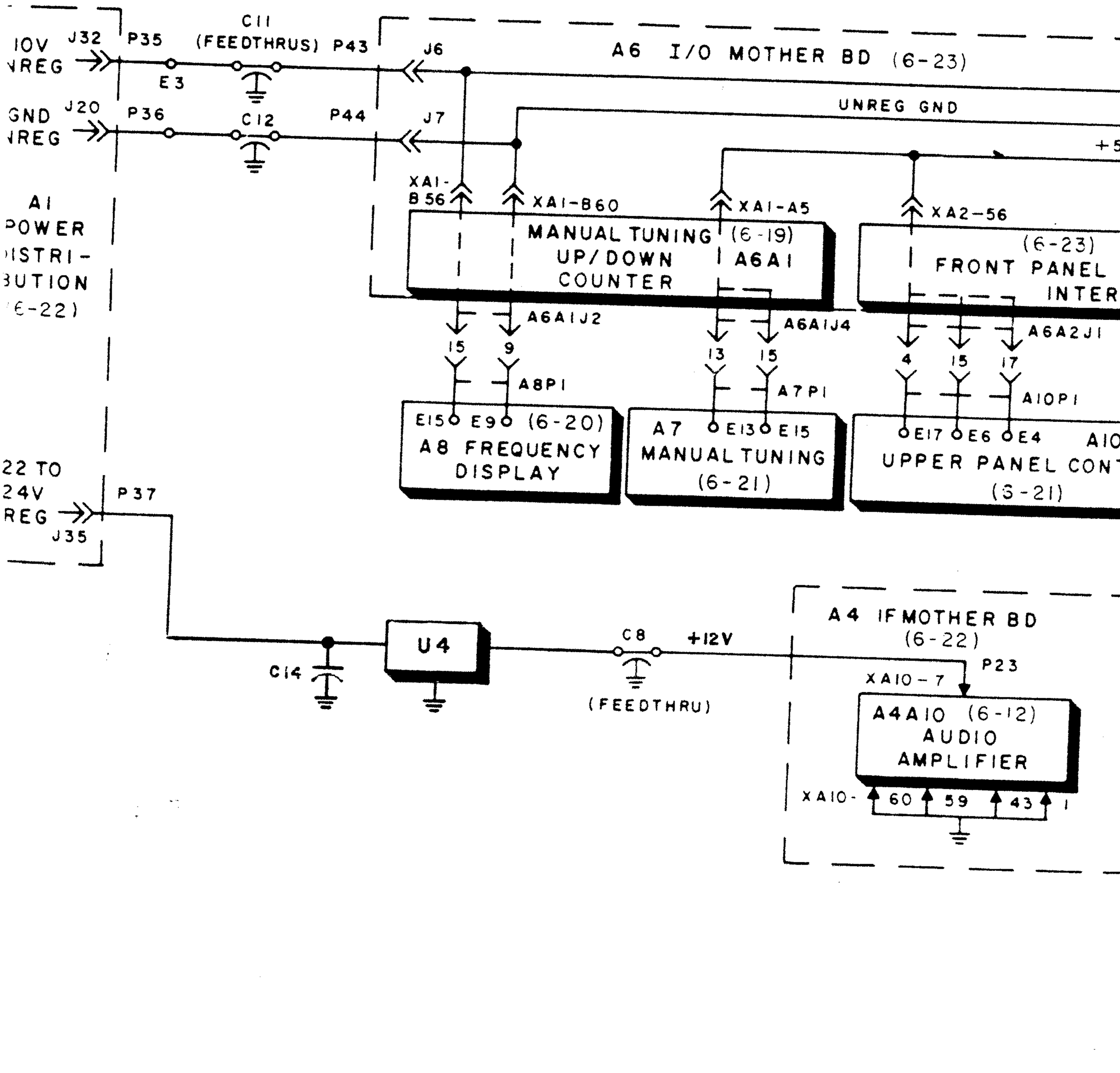


Figure 3-5. Power Supply Voltage Distribution I
(Sheet 3 of 3)


10V UNREG
J32
P35
E3
C11 (FEEDTHRUS)
P43
J6
A6 I/O MOTHER BD (6-23)
GND UNREG
J20
P36
C12
P44
J7
UNREG GND
+5
A1 POWER DISTRI-BUTION (6-22)
XA1-B56
XA1-B60
XA1-A5
XA2-56
MANUAL TUNING UP/DOWN COUNTER
(6-19)
A6A1
(6-23)
FRONT PANEL INTER
A6A1J2
A6A1J4
A6A2J1
15
9
13
15
4
15
17
A8P1
A7P1
A10P1
E15 E9 (6-20)
A8 FREQUENCY DISPLAY
A7 E13 E15
MANUAL TUNING
(6-21)
E17 E6 E4
UPPER PANEL CON
(6-21)
22 TO 24V REG
J35
P37
C14
U4
C8
+12V
(FEEDTHRU)
A4 IF MOTHER BD
(6-22)
P23
XA10-7
A4A10 (6-12)
AUDIO AMPLIFIER
XA10-
60
59
43
1

3.4.1 TYPE 791616-1 RF INPUT FILTER (A2)

Within this assembly is a Type 280093 PC board which contains the circuitry of the RF input filter. The schematic diagram for this circuit is **Figure 6-1.** The circuit is a 15-pole, elliptic function low-pass RF filter, with an insertion loss of less than 3.5 dB over normal input range of 5 kHz to 30 MHz. Above 30 MHz, the attenuation increases rapidly. This attenuation improves the image rejection and reduces the conducted LO leakage of the receiver. Over the range of LO and image frequencies, the attenuation of the input filter exceeds 80 dB. Resistor R1 provides a dc path to ground to bleed off any accumulated static charge at the RF input. Diodes CR1 through CR4 use the Zener breakdown potential to protect the rest of the receiver from input signals in excess of +15 dBm. C12 and L1 provide a high frequency trap to prevent radiation of harmonics of the 1st LO. The nominal input impedance of the filter is 50 Ω.

3.4.2 TYPE 791592-1 INPUT CONVERTER (A3)

Figure 3-6 is a detailed functional block diagram of the Input Converter which should be referred to in the following circuit description. **Figure 6-2,** Input Converter Schematic Diagram, may be referred to for greater component level detail, if desired.

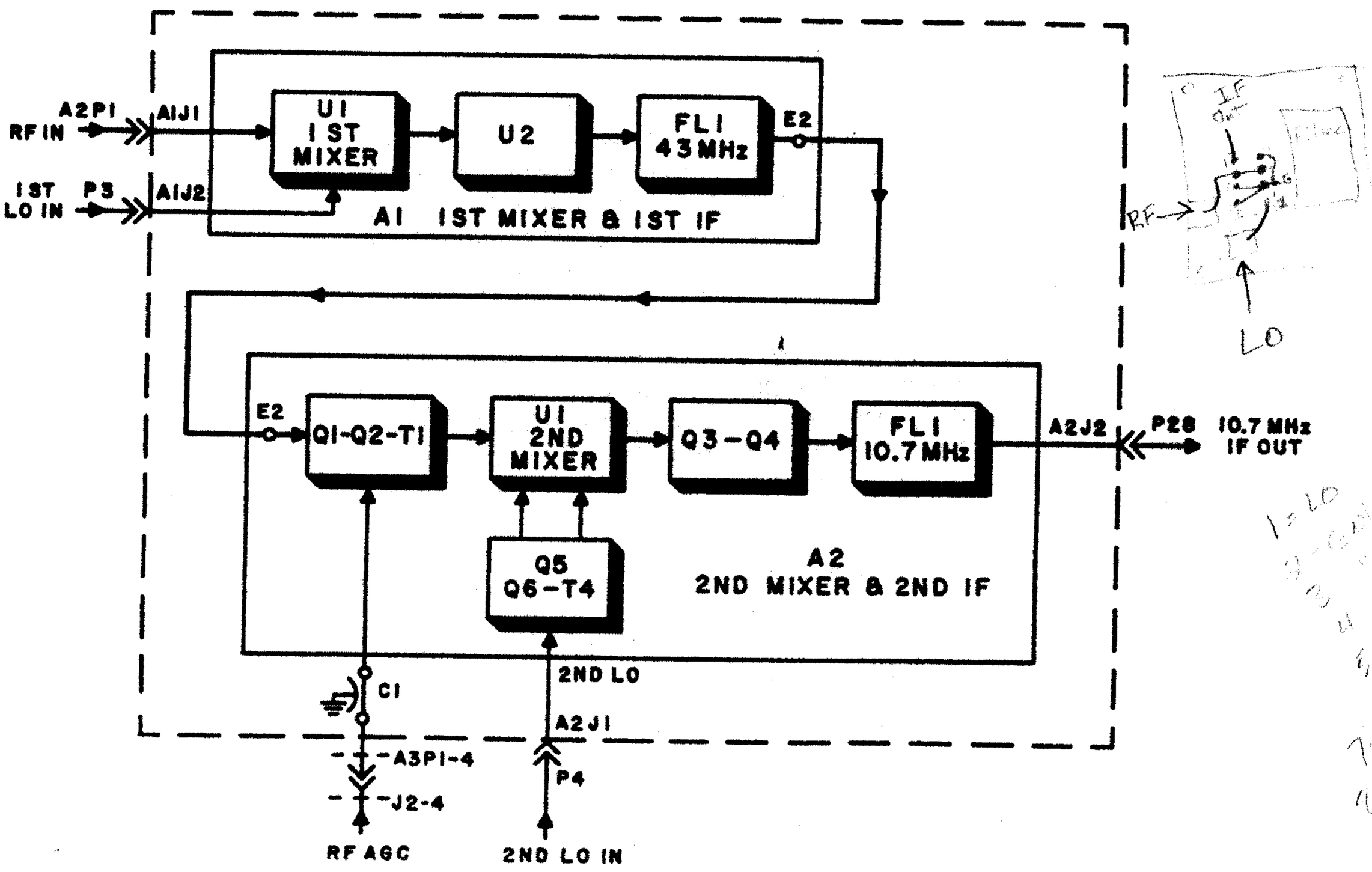


Figure 3-6. Input Converter Functional Block Diagram.

3.4.2.1 Circuit Description

All signals entering the Input Converter from the RF Filter are converted up in frequency and filtered. Signals passed by the 1st IF Filter are amplified and converted down in frequency to 10.7 MHz. Here they are further amplified and filtered. The overall net gain of the Input Converter is roughly +17 dB when zero gain control current is applied.

Signals reaching the 1st Mixer, A1U1, may be any frequency from 5 kHz up to slightly above 30 MHz and any level from the noise floor to +30 dBm. In general, many signals will be present covering a wide range of levels. The role of the 1st Mixer is to handle these in such a way that the balance of the receiver can select the desired signal and reject all others. To accomplish this, a high level mixer is used and relatively high (+20 dBm) local oscillator power is applied. The conversion loss of the 1st Mixer is approximately 6 dB. Therefore, the 1st Mixer is followed by amplifier A1U2 to restore the signals to their original levels. A1U2 is a broadband hybrid integrated amplifier with a low noise figure, a good terminating impedance for the mixer, and a large signal handling ability.

The output load of A1U2 is 50 Ω, ensuring a proper driving impedance for the 1st IF crystal filter A1FL1. This filter requires a 50 Ω source and load and has a center frequency of 42.905 MHz and a 3 dB bandwidth of 28 kHz. The primary function of A1FL1 is to reject unwanted signals which are passed by the RF Filter and 1st Mixer and to establish the initial IF bandpass.

Signals passed by A1FL1 are coupled to a second amplifier, A2Q2, through a coupling network. This amplifier has a similar constant current source A2Q1 biasing it. Its output circuit is a broadly tuned transformer, but is shunted by gain control diode A2CR2. As the current through the diode increases, its RF impedance decreases and the net gain of A2Q2 is decreased. Current to A2CR2 is supplied by the RF Gain portion of the AGC, A4A6. As the current varies from zero to maximum, there is approximately 30 dB of gain reduction.

The output signal of A2Q2 is down converted by the 2nd Mixer, A2U1. The 2nd LO signal enters the Input Converter via A2J1 at a level of approximately 0 dBm. Common emitter amplifiers, A2Q5 and A2Q6, provide enough gain to bring the 2nd LO signal to a nominal level of +17 dBm. Each of these stages is broadly tuned transformer-coupled and each has some unbypassed emitter resistance to preserve a relatively low harmonic content in the 2nd LO signal.

The 2nd Mixer is followed by a bipolar cascode amplifier. It consists of common emitter stage A2Q4 and common base stage A2Q3. These provide relatively high gain with good stability and low noise contribution. Transformer A2T2 couples the output of A2Q3 to crystal filter A2FL1. This filter has a center frequency of 10.7 MHz, a bandwidth of 16 kHz, and requires 50 Ω terminations.

The received signal frequency which corresponds to the center of the 2nd IF at exactly 10.7 MHz depends on the frequencies of both the 1st and 2nd LOs. The control of these two oscillators is described in the Synthesizer Section 3.3.

3.4.3 TYPE 791569-1 IF MOTHERBOARD (A4)

The schematic diagram of the IF Motherboard is **Figure 6-3.** The IF Motherboard has 11 positions for plug-in circuit cards. A total of 10 positions are used and the eleventh is a spare.

FIGURE 3-7

3.4.4 TYPE 791594-1 10.7 MHz FILTER SWITCH (A4A1)

Figure 3-7 is a detailed functional block diagram of the 10.7 MHz Filter Switch which should be referred to in the following circuit description. **Figure 6-4**, 10.7 MHz Filter Switch Schematic Diagram, may be referred to for greater component level detail, if desired.

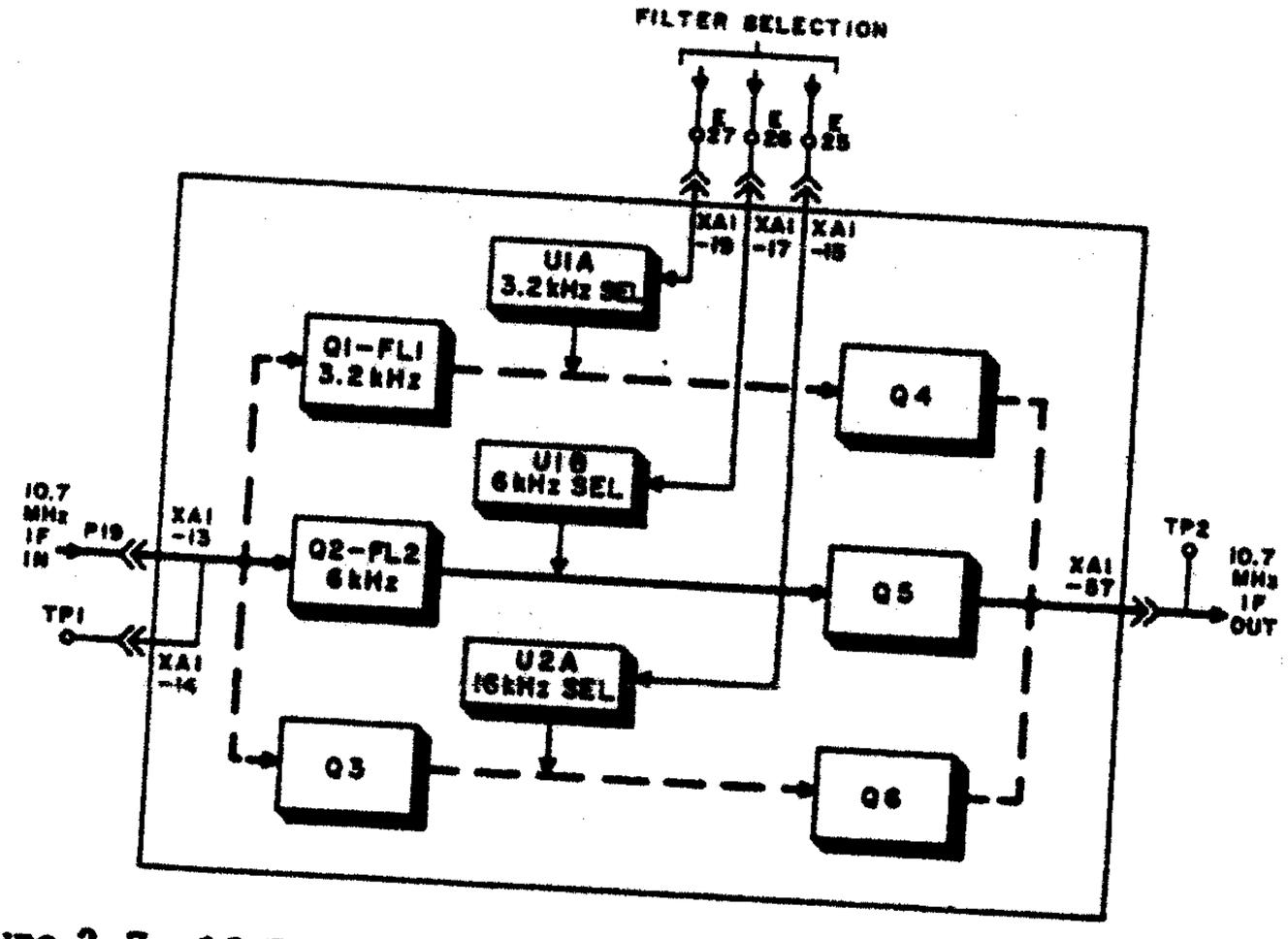


Figure 3-7. 10.7 MHz Filter Switch Functional Block Diagram.

3.4.4.1 Circuit Description

The 10.7 MHz Filter Switch receives the 10.7 MHz IF signal output from the Input Converter, A3. At this point, the IF bandwidth has been set at 16 kHz by a filter in the Input Converter. The 10.7 MHz Filter Switch contains bandpass filters of 6 kHz and 3.2 kHz bandwidth. The purpose of this circuit is to route the IF signal through one of these filters, or through a wideband path which allows the full 16 kHz bandwidth to pass. The selection of the filter path is made by application of a logic high level to one of the three control terminals.

In any IF bandwidth, a logic high is applied to one of three control lines from the I/O Motherboard, at pin 15, 17, or 19. These lines are connected to the non-inverting inputs of U1A, U1B, and U2A. The inverting inputs are held at approximately 0.8 V by voltage divider R52-R53. The output voltage of the selected op-amp swings positive, turning on one pair of common-emitter IF amplifier stages. For example, if U1A is selected, Q1 and Q4 are turned on.

The 10.7 MHz IF signal is input at pin 13 and coupled through C1 to the base circuits of Q1, Q2, and Q3. If Q1 is on, the signal is amplified and coupled to FL1. This filter has a 200 Ω input impedance and a 3 dB bandwidth of 3.2 kHz. The filtered IF signal is applied to amplifier Q4 through level-adjust potentiometer R26. The amplified IF signal is output at pin 57. If 6 kHz bandwidth is selected, the IF signal is routed through Q2, FL2, and Q5. If any other bandwidth is selected, the IF signal is routed through Q3, attenuator R22, R23, R24, and Q6. The gain of the three signal paths is equalized by R26, R28, and R30 to approximately dB. The circuit has nominal input and output impedances of 50 Ω.

3.4.5 TYPE 71430-1 10.7 MHz/455 kHz CONVERTER (A4A2)

Figure 3-8 is a detailed functional block diagram of the 10.7 MHz/455 kHz Converter which should be referred to in the following circuit description. **Figure 6-5,** 10.7 MHz/455 kHz Converter Schematic Diagram, may be referred to for greater component level detail, if desired.

3.4.5.1 Circuit Description

The 3rd Mixer converts signals from 10.7 MHz to 455 kHz. The 3rd LO signal is input at the fixed frequency of 11.155 MHz and a level of approximately -6 dBm, and is amplified by transistor Q1 and its associated circuitry to +7 dBm before entering the mixer. The amplifier operates as a common emitter stage with some unbypassed emitter resistance to stabilize its gain and reduce distortion. The pi-network, C7-L2-C8, serves as an impedance transformer and low-pass filter, further reducing distortion of the LO signal.

Low-pass filter C9, L3, C10, L4, and C11 filters out undesired components above 500 kHz from the mixer output and matches impedances between the mixer and the following circuits. The nominal input impedance of the 3rd Mixer is 50 Ω and the output impedance is 1000 Ω.

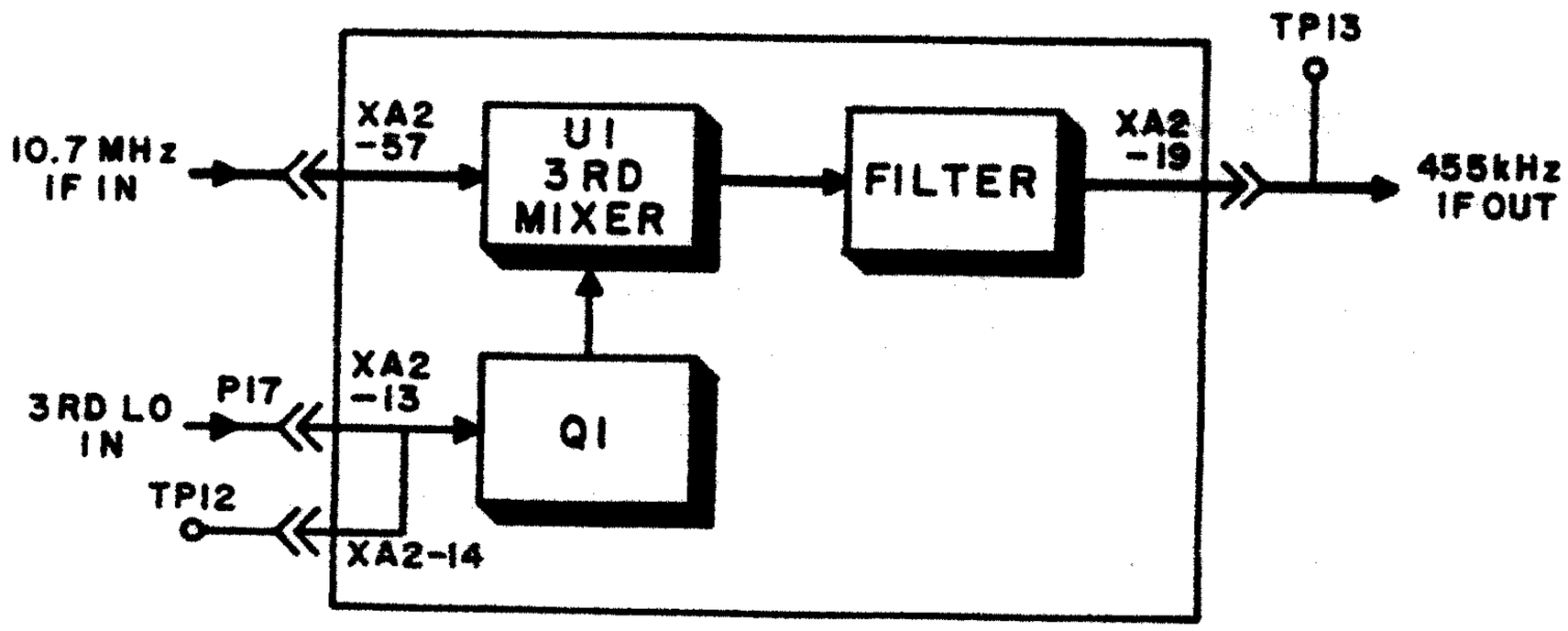


Figure 3-8. 10.7 MHz/455 kHz Converter Functional Block Diagram.

3.4.6 TYPE 791595-1 455 kHz FILTER SWITCH (A4A3)

Figure 3-9 is a detailed functional block diagram of the 455 kHz Filter Switch which should be referred to in the following circuit description. **Figure 6-6,** 455 kHz Filter Switch Schematic Diagram, may be referred to for greater component level detail, if desired.

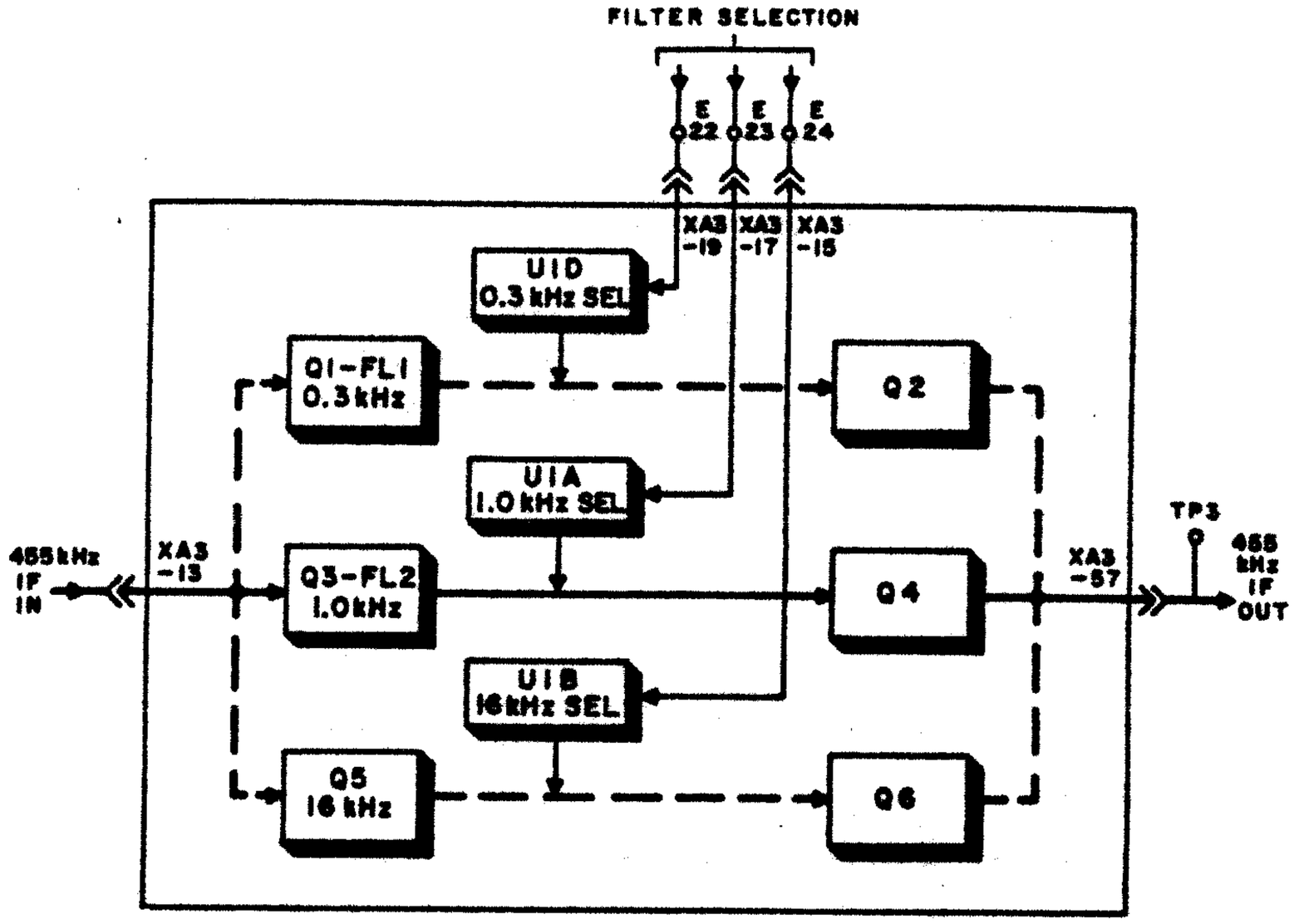


Figure 3-9. 455 kHz Filter Switch Functional Block Diagram.

3.4.6.1 Circuit Description

The 455 kHz Filter Switch is similar in function to the 10.7 MHz Filter Switch. Both contain three possible signal paths, two with crystal filters and one with broad bandwidth. There are, however, several important differences between the two filter switches. The 455 kHz bandwidth is 0.3 kHz when Q1 and Q2 are activated, and 1 kHz when Q3 and Q4 are activated. When Q5 and Q6 are activated the broad bandwidth path is energized, thus allowing the overall receiver bandwidth to be controlled by the 10.7 MHz Filter Switch or the Input Converter. In the 455 kHz Filter Switch it is possible for all paths to be off when the USB or LSB filters are selected.

The input signal at pin 13 connects in parallel to Q1, Q3, and Q5. When Q1 is biased on, the signal passes through Q1 and is fed through the 0.3 kHz crystal filter (FL1). The biasing of Q1 and Q2 is controlled by the voltage on pin 19. When this voltage is high (+5 V), the output of U1D will be +12 V, thus biasing Q1 and Q2. When this voltage is low (0 V), the output of U1D will be -12 V which will cause an approximate 1 V reverse bias to the bases of Q1 and Q2, and thus they are turned off.

When the 1 kHz bandwidth is selected, module pin 17 is high, and U1A turns on Q3 and Q4. When the 3.2 kHz, 6 kHz, or 16 kHz bandwidths are selected, module pin 15 is high and U1B turns on Q5 and Q6. When ISB, LSB, or USB are selected, all three control lines to this card are low and all three signal paths are inhibited.

All transistors, Q1 through Q6, are operated as common emitter amplifiers with unbypassed emitter resistors to control their gain. Through any of the three signal paths there is a net voltage gain of approximately 9 dB from the input to the output of the module. OP

AMP section U1C is not used and is as shown in the schematic connected in an inoperative condition.

3.4.7 TYPE 791596-1 USB FILTER SWITCH (A4A4) (Optional in WJ-8718/8718-9)

Figure 3-10 is a detailed functional block diagram of the USB Filter Switch which should be referred to in the following circuit description. **Figure 6-6**, USB Filter Switch Schematic Diagram, may be referred to for greater component level detail, if desired.

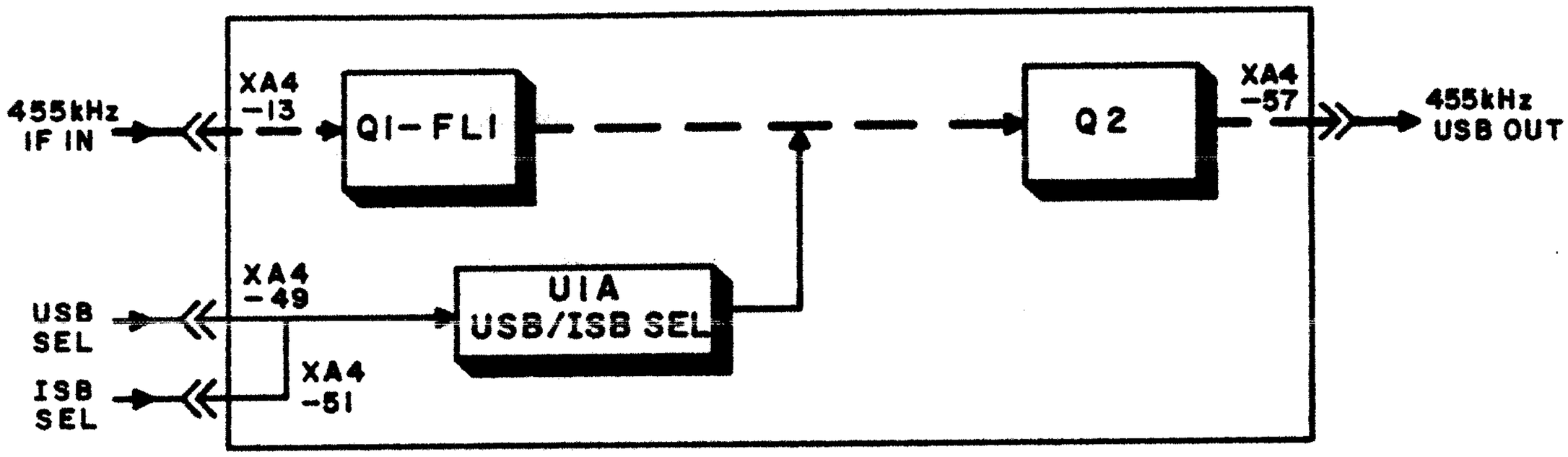


Figure 3-10. USB Filter Switch Block Diagram.

3.4.7.1 Circuit Description

The USB Filter Switch input, pin 13, connects into the 455 kHz IF signal path, in parallel with the 455 kHz Filter Switch. When the receiver is operating in either the USB mode or the ISB mode, the upper sideband modulation is passed in this circuit and sent to the 455 kHz Amplifier/AM Detector (A4A7). The upper sideband filter (FL1) has a bandpass extending from 455.25 kHz to 458.2 kHz.

When either the USB or ISB detection mode is selected, a logic high is applied to the non-inverting input of U1A. This causes its output voltage to swing to near +15 V. The switching threshold (approximately 1.6 V) is set by R17 and R18. The positive output voltage supplies bias current to amplifiers Q1 and Q2, turning them on. The 455 kHz IF signal, with 16 kHz bandwidth, is amplified by Q1 and applied to the upper sideband filter, FL1. The upper

sideband is amplified by Q2 and output via pin 57. Potentiometer R23 provides gain adjustment for equalizing the USB signal level with the other filtered IF signals. Resistors R7 and R8 provide impedance matching for the filter input and output, respectively.

3.4.8 TYPE 791597-1 ISB/LSB FILTER SWITCH (A4A5) (Optional in WJ-8718/8718-9)

Figure 3-11 is a detailed functional block diagram of the ISB/LSB Filter Switch which should be referred to in the following circuit description. **Figure 6-7**, ISB/LSB Filter Switch Schematic Diagram, may be referred to for greater component level detail, if desired.

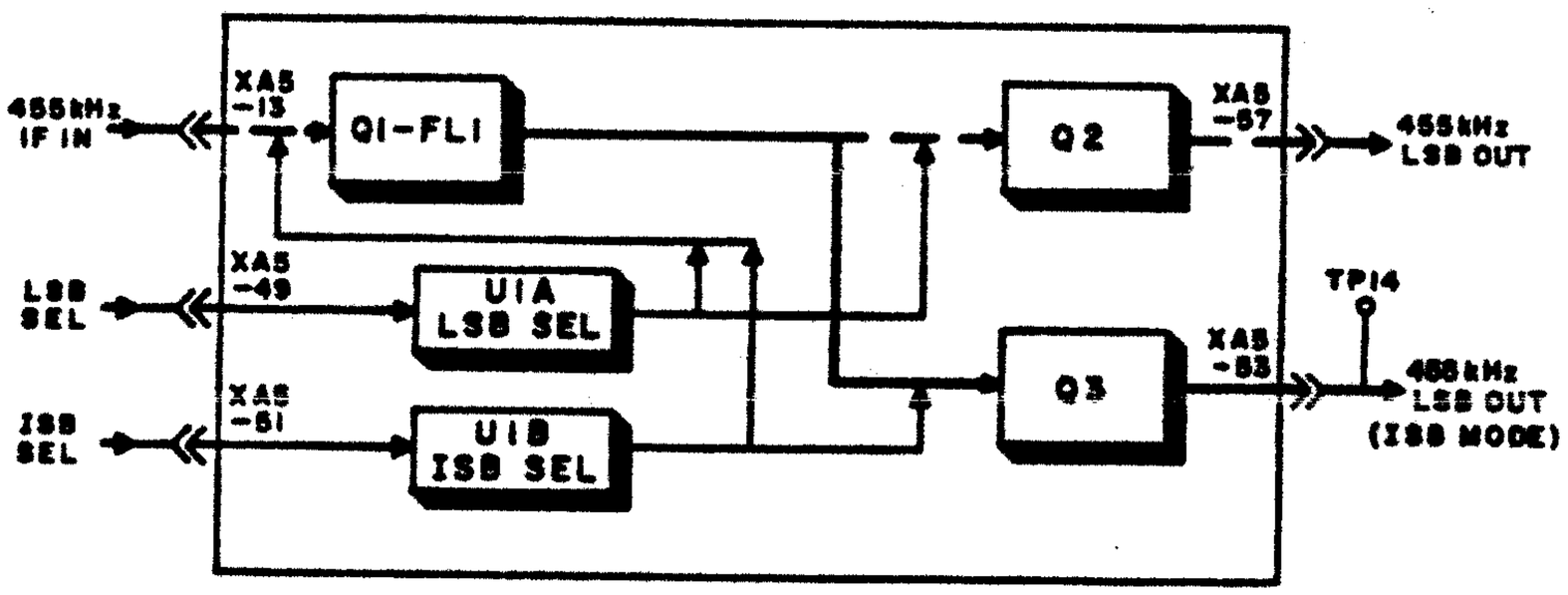


Figure 3-11. ISB/LSB Filter Switch Functional Block Diagram.

3.4.8.1 Circuit Description

The ISB/LSB Filter Switch input, pin 13, connects into the 455 kHz IF signal path, in parallel with the 455 kHz Filter Switch. The circuit has two signal outputs, one to the 455 kHz Amplifier/AM Detector (A4A7), and one to the ISB Detector and Audio (A4A8). When the receiver is operating in the LSB detection mode, the lower sideband modulation is output to the 455 kHz Amplifier/AM Detector (A4A7). When the receiver is in the ISB detection mode, the lower side modulation is output to the ISB Detector and Audio board. The lower sideband filter (FL1) has a bandwidth extending from 451.8 kHz to 454.75 kHz.

When the LSB Detection mode is selected, a logic high is applied to the non inverting input of U1A. This causes the output voltage to swing to near +15 V. The switching threshold (approximately 2.5 V) is set by R23 and R24. Diode CR1 conducts, supplying bias current through R15 to turn on IF amplifier Q1. Output amplifier Q2 is also biased on, but current flow in R21 and R9. The 455 kHz IF signal, with 16 kHz bandwidth, is amplified by Q1 and applied to the lower sideband filter, FL1. The lower sideband is amplified by Q2 and output via pin 57.

When ISB detection mode is selected, Q1 is biased on by U1B and CR2, as previously described. Output amplifier Q3 is also biased on by current flow in R26 and R27. The lower-sideband information is amplified by Q3 and output via pin 53. Notice that only one output amplifier is operating in either mode. Potentiometer R32 allows gain adjustment for equalizing the filtered IF signal levels. Resistor R8 provides input impedance matching for the filter, and the output impedance is matched by R9 and R27.

3.4.9 TYPE 78112-1 AGC AMPLIFIER (A4A6)

Figure 3-12 is a detailed functional block diagram of the AGC Amplifier which should be referred to in the following circuit description. **Figure 6-9**, AGC Amplifier Schematic Diagram, may be referred to for greater component level detail, if desired.

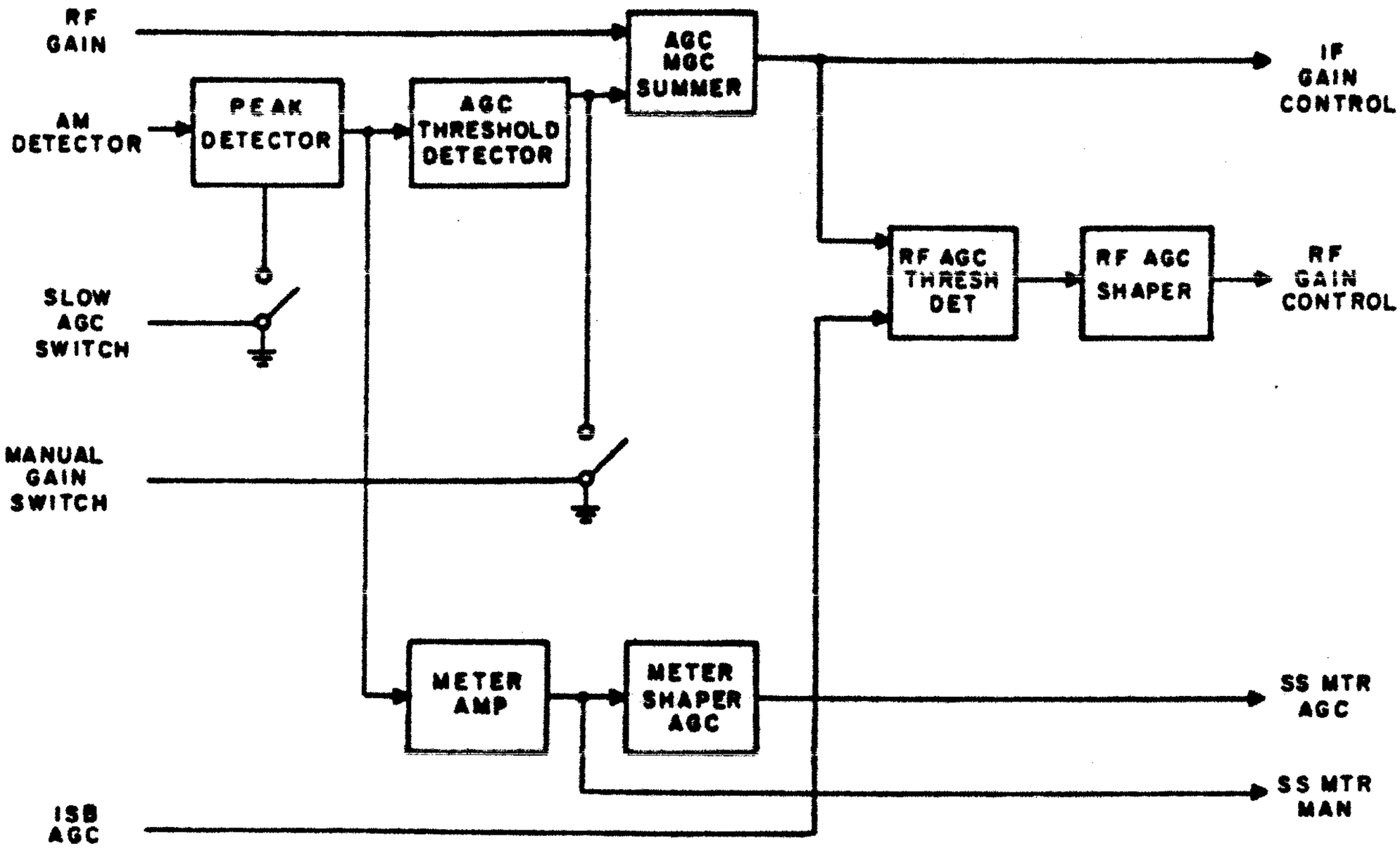


Figure 3-12. AGC Amplifier Functional Block Diagram.

3.4.9.1 **Circuit Description**

The primary function of the AGC Amplifier is to generate control voltages which adjust the amplification of signals passing through the receiver. When the Fast AGC or Slow AGC gain mode is selected, this module adjusts the receiver amplification (gain) to maintain a constant output from the AM Detector. If the desired signal entering the receiver should fade in amplitude, the receiver gain will increase just enough to compensate for the fade. When Manual gain mode is selected, the receiver gain is fixed at a level which depends on the setting of the RF Gain potentiometer on the front panel. This module, as a secondary function, provides voltage to operate the signal strength meter.

The differences in decay times of Fast AGC and Slow AGC make them useful for different kinds of signals. In the Fast AGC mode, the gain of the receiver adjusts about as quickly for a rise in signal strength as it does for a fall in signal strength. The time taken to respond to a rise is referred to as attack time, and the time taken for a fall is known as decay time. The response to rising signals remains fast in the Slow AGC mode, but when the signal strength falls the change in gain occurs much slower. For AM and FM signals, the total power contained in the carrier and sidebands does not vary much with time at the transmitter. With these types of signals, the main purpose of the AGC is to compensate for atmospheric losses between transmitter and receiver. These changes occur slowly or rapidly as several rises and falls per second. For signals of this sort, the characteristics of the Fast AGC mode will serve best. However, for pulsed signals such as telegraphy (A1 emission) and for SSB voice signals (A3J emission) there are rapid fluctuations in transmitted power with recurring peaks. When this type of signal is received, it is usually desirable that the AGC have a sort of memory for the peaks but still be able to respond quickly if there is an abrupt increase in signal level. Hence, the fast attack and slow decay times of the Slow AGC is desired for these cases.

There will also be instances where it is desirable to fix the gain of the receiver at some value to make critical comparisons of signal strength or to eliminate signals or noise below a particular amplitude. For these cases, the Manual gain mode is useful. When using this mode, it is desirable to adjust the RF GAIN control so the signal strength meter reads at the MAN SET line for the average signal to be monitored, to obtain the greatest latitude for signal level change.

In the AGC module, the direct coupled output of the AM detector is filtered by R5 and C3 to limit the speed of response of the Fast AGC. In the Fast AGC Mode, Q7 is biased off, disconnecting C4, so Q1 operates simply as an emitter follower. Q7 is biased on when Slow AGC is selected, grounding the negative end of C4. In this case Q1 can charge C4 quickly if there is a rise in input from the AM Detector, but when the input falls below its peak value Q1 is turned off by the charge stored in C4. Q1 continues to be off until C4 is discharged by R3. This action gives the fast attack response and slow decay response of the Slow AGC mode. Zener diode CR2 acts as a limiter to prevent short bursts of signal from overcharging C4 (which might cut off the amplifiers for many seconds).

OP AMP U1A acts as a buffer between C4 and the following circuits. A general-purpose diversity AGC output is provided at pin 16. Transistor Q2 acts as a threshold detector, blocking AGC action for weak signals. This is desirable to allow a maximum signal-to-noise ratio to be obtained in all stages of the receiver before any gain reduction is permitted. The base of Q2 is biased to approximately +0.2 V. If the emitter of Q2 is lower than about +0.8 V, Q2 will be turned off and no AGC action can occur. When the output of U1A is greater than +0.8 V, Q2 conducts and a gain control voltage appears across R13. When the Manual gain mode is selected, Q3 and Q6 will be turned on and will clamp the voltage on R13 to ground, and +5 V

will be applied to the RF Gain potentiometer on the front panel. OP AMP U2B acts as an inverting summing amplifier for the voltage at R13 (which will be zero in Manual gain mode) and the voltage on the RF GAIN control (which will be zero in Fast or Slow AGC modes).

The output of summing amplifier U2B is buffered by OP AMP U1D and fed to the 455 kHz amplifier on A4A7. Zero volts from U1D allows the 455 kHz amplifier to operate at maximum gain while a negative output from U1D causes the gain of the IF amp to be reduced.

A sample of the IF gain control voltage from U2B is also applied to RF AGC threshold detector Q5. This threshold detector causes the gain reduction to occur only in the 3rd IF amplifier, unless the signal at the RF input of the receiver and in the early stages of the receiver is great enough to ensure a good signal-to-noise ratio even in the early stages. The operation of the threshold detector is the same as that of Q2, except with polarities reversed to allow for the inversion which occurs in U2B. The base of Q5 is biased around -2.7 V so the IF gain control voltage must be more negative than -3.3 V for Q5 to conduct. When the ISB Detector and Audio module (A4A8) is installed and energized (ISB mode only), a similar AGC circuit in that module supplies a corresponding sample of its IF gain control voltage to Q4. This allows the RF gain control to respond to either the USB component, amplified by A4A7, or the LSB component, amplified by A4A8. This combined action is necessary to protect against possible overload of the 1st and 2nd IF which are common to both USB and LSB. Q4 duplicates the operation of Q5. When the ISB module is not installed or not selected, Q4 does not conduct and may be ignored.

As stated in the description of the Input Converter, the gain control in the 1st IF amplifier is accomplished by varying the RF impedance of a diode that shunts the load circuit of one stage. The impedance of this diode is approximately inversely proportional to the dc current through it. Therefore, to obtain a 6 dB gain reduction requires a certain current, an additional 6 dB reduction requires doubling the current and another 6 dB reduction requires four times the original current and so on. To achieve the desired relationship between AM Detector output and RF gain reduction requires that the control diode current rise slowly at first, then more rapidly as the received signal strength increases further (exponentially). This current/voltage relationship is obtained through a shaping network comprised of U2D, R47, R48, CR5, and R31. The actual current for the control diode is supplied by buffer U2A.

The relationship between signal strength and the voltage out of U1A make this voltage suitable for operation of the signal strength meter. In the Manual gain mode, this voltage is proportional to the RF input signal voltage. Its polarity is inverted by OP AMP U1C and it is applied through R49 and front panel switches A10A1S1B and S2C to the meter. This allows the receiver to act as a tuned voltmeter whose calibration depends on the setting of the RF GAIN control.

In the AGC modes, the voltage out of U1A increases approximately linearly with signal voltage up to the AGC threshold level of 3 μV (RF input). Above this level the U1A output is compressed by AGC action to be nearly proportional to the logarithm of the RF input voltage. By using a shaping network composed of R41, R50, R51, CR6, CR7, and CR8 to suitably compress the output of U1C at low signal levels, the signal strength meter is made to be approximately linear in dB over a greater than 100 dB range. Resistors R50 and R51 control the amount of compression and the exact fit of the meter scale with signal strength. If an accurate source of variable signal level is available, these fixed resistors may be replaced with variable ones which may be adjusted for best tracking of the meter. The variable resistors may then be removed, measured and replaced with fixed resistors of the same value.

3.4.10 TYPE 72488-1 455 kHz AMPLIFIER/AM DETECTOR (A4A7)

Figure 3-13 is a detailed functional block diagram of the 455 kHz Amplifier/AM Detector which should be referred to in the following circuit description. **Figure 6-10**, 455 kHz Amplifier/AM Detector Schematic Diagram, may be referred to for greater component level detail, if desired.

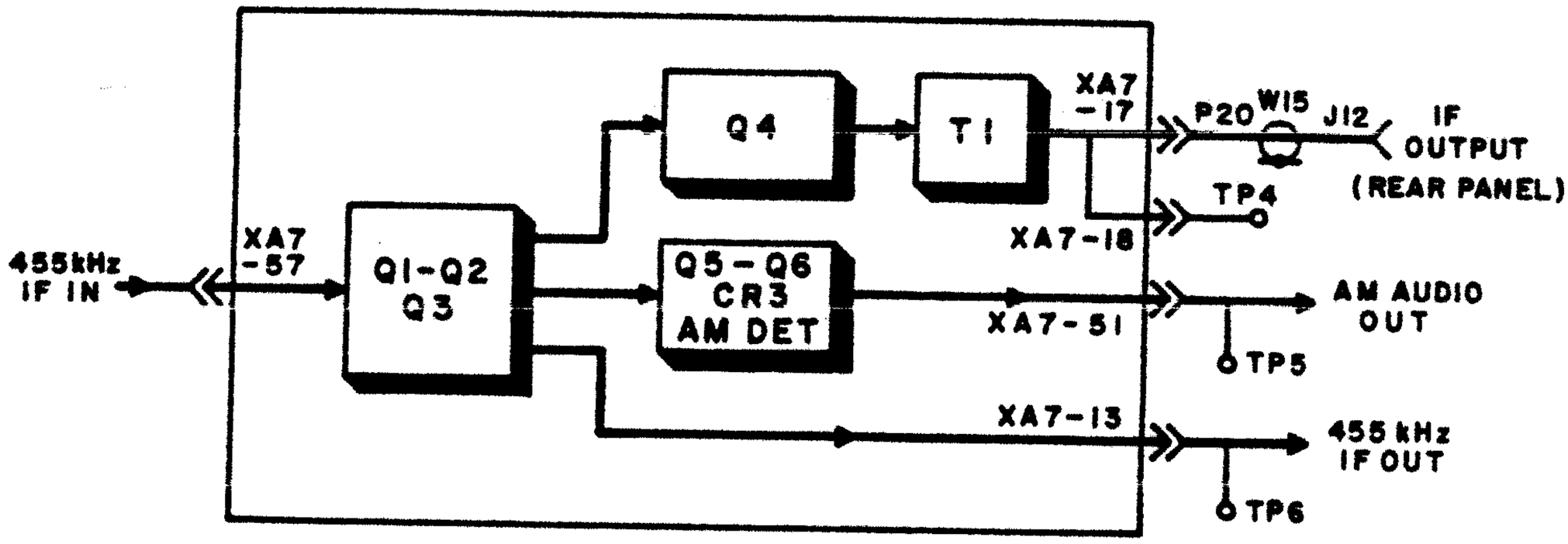


Figure 3-13. 455 kHz Amplifier/AM Detector Functional Block Diagram.

3.4.10.1 Circuit Description

Although received signals are amplified by most of the circuits in the receiver, the majority of the amplification of weak signals takes place in the 455 kHz amplifier of A4A7. Following a two-stage gain controlled amplifier, the input signal is split to provide three outputs: the IF sample which operates the FM/CW/SSB Demodulator, the IF output for the rear panel, and the input to the AM Detector. The AM Detector, which operates at a relatively high level for good linearity, has its output directly coupled to the AGC module and the Audio Amplifier.

FET's Q1 and Q2 operate as common source amplifiers with their gains controlled by a variable voltage applied to gate 2 of each transistor. Inductor L1 broadly tunes the output of Q1 by cancelling any stray capacitance, but the network consisting of L2, C9, C10, C11, and L3 forms a double-tuned bandpass filter of approximately 35 kHz bandwidth. This filter is narrow enough to suppress any broadband noise contributed by earlier stages of the receiver, but at the same time is wide enough not to restrict the receiver's bandwidth. Potentiometer R7 between the first and second amplifiers adjusts the maximum gain of the amplifiers and hence of the whole receiver.

Transistor Q3 serves as a buffer between the 455 kHz amplifier and its three outputs. For signals fed to the FM/CW/SSB Detector (pin 13), Q3 acts as an emitter-follower stage. For the rear panel IF Output, Q3 feeds the signal to Q4, which acts as a power amplifier. Transformer T1 supplies a 50 Ω IF output to the rear panel, providing a nominal 20 mV IF output for RF inputs greater than 3 μV. For the AM detector, Q3 and Q5 both act as common-emitter

amplifiers to raise the IF signal to a level of several volts which will permit the detector diode, CR3, to perform linearly. Diodes CR4 and CR5 provide a dc-bias to operate the AM Detector and emitter-follower (Q6) above ground to establish the proper dc level for the AGC circuit. The low-pass filter of L7 and C28 suppresses any residual IF signal.

3.4.11 TYPE 791598-1 ISB DETECTOR/AUDIO (A4A8) (Optional in WJ-8718/8718-9)

Figure 3-14 is a detailed functional block diagram of the ISB Detector/Audio which should be referred to in the following circuit description. **Figure 6-11**, ISB Detector/Audio Schematic Diagram, may be referred to for greater component level detail, if desired.

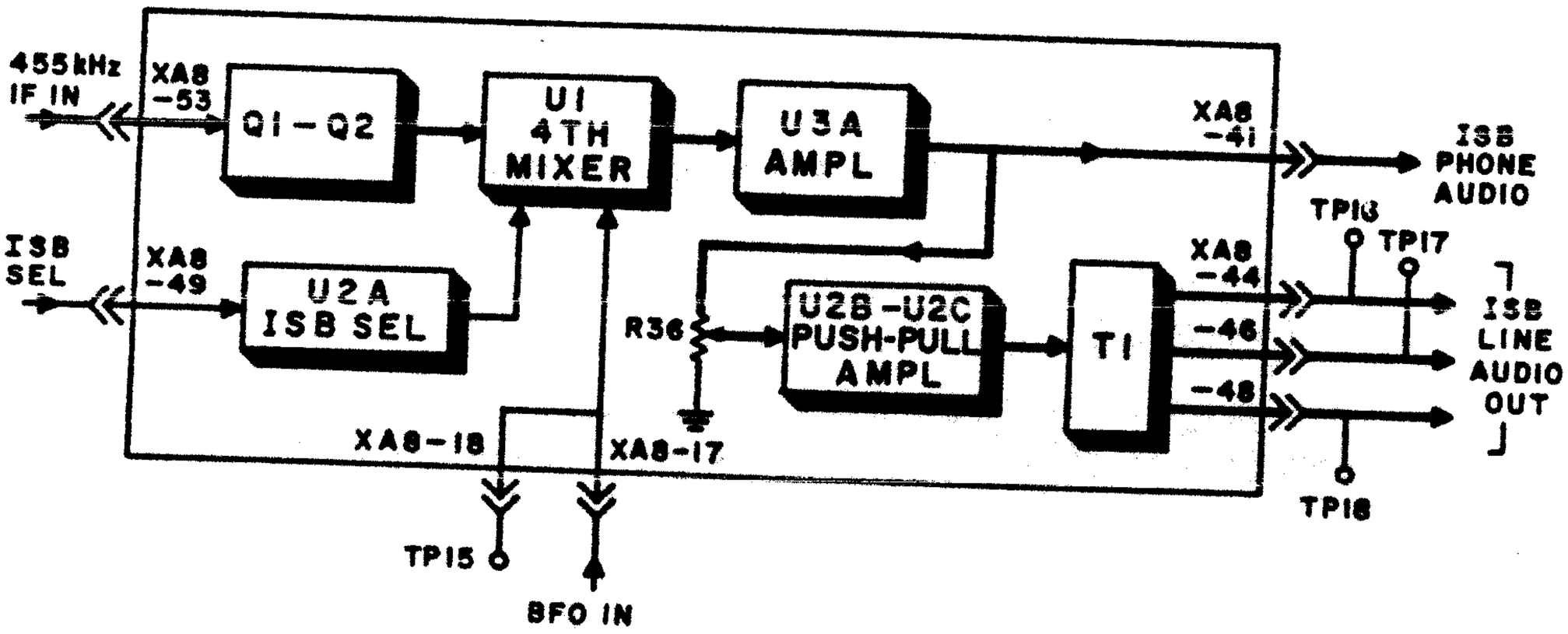


Figure 3-14. ISB Detector/Audio Functional Block Diagram.

3.4.11.1 Circuit Description

For ISB operation, two independent single sideband signals must be demodulated. Since they share the same carrier frequency, they may be processed together up to a certain point. In this receiver, ISB is handled as a single composite signal through the 3rd Mixer. At that point it is split, the USB component being filtered and passed through the main signal path, the LSB component filtered and separately amplified and demodulated by the ISB Detector and Audio module.

The ISB Detector and Audio module is therefore a combination of circuits from other modules previously discussed. There is a 455 kHz amplifier similar to part of A4A7, a product detector similar to that on A4A9, an AGC circuit like part of A4A6, and an ISB line audio amplifier similar to the auxiliary phone amplifier on A4A10. A sample of the AGC voltage developed in this module is sent to the main AGC module to produce a combined RF AGC.

Common source FET amplifiers Q1 and Q2 have variable gain depending on their gate 2 voltage. This voltage is derived from the module's AGC section. Potentiometer R8 is used to set the maximum gain of the amplifier to give the same input level to balanced modulator U1 as is received by A4A9U2 at low signal levels.

Balanced modulator U1 uses the BFO to act as a 4th Mixer and converts the LSB signal to audio. When the ISB mode is selected, +5 V is applied to pin 49 and U2A switches on, supplying power to U1. Its output is low-pass filtered and then amplified by U3A. The output of U3A splits three ways. It leaves the module to go to the front panel which provides LSB phone audio in the ISB mode. It also feeds the ISB Line Audio amplifier through level control R36, and drives the AGC circuit.

The AGC is a simplified form of the one on A4A6. It always acts in the Slow AGC mode. Peak detector Q4 charges C19, which discharges through R52. Buffer U2D drives AGC threshold detector Q3. The output of Q3 is amplified by U3D to supply the IF AGC to amplifiers Q1 and Q2 via buffer U3C, and the sample to the RF AGC circuit on A4A6. When the ISB mode is selected, Q5 is turned off by the positive output from U2A. No meter outputs are supplied by this module.

The ISB Line Audio amplifier (U2B and U2C) is identical, except for component values, to the auxiliary phone amplifier on A4A10, which will be discussed in detail in **paragraph 3.4.13.**

3.4.12 TYPE 791599-1 FM/CW/SSB DETECTOR (A4A9)

Figure 3-15 is a detailed functional block diagram of the FM/CW/SSB Detector which should be referred to in the following circuit description. **Figure 6-12,** FM/CW/SSB Detector Schematic Diagram, may be referred to for greater component level detail, if desired.

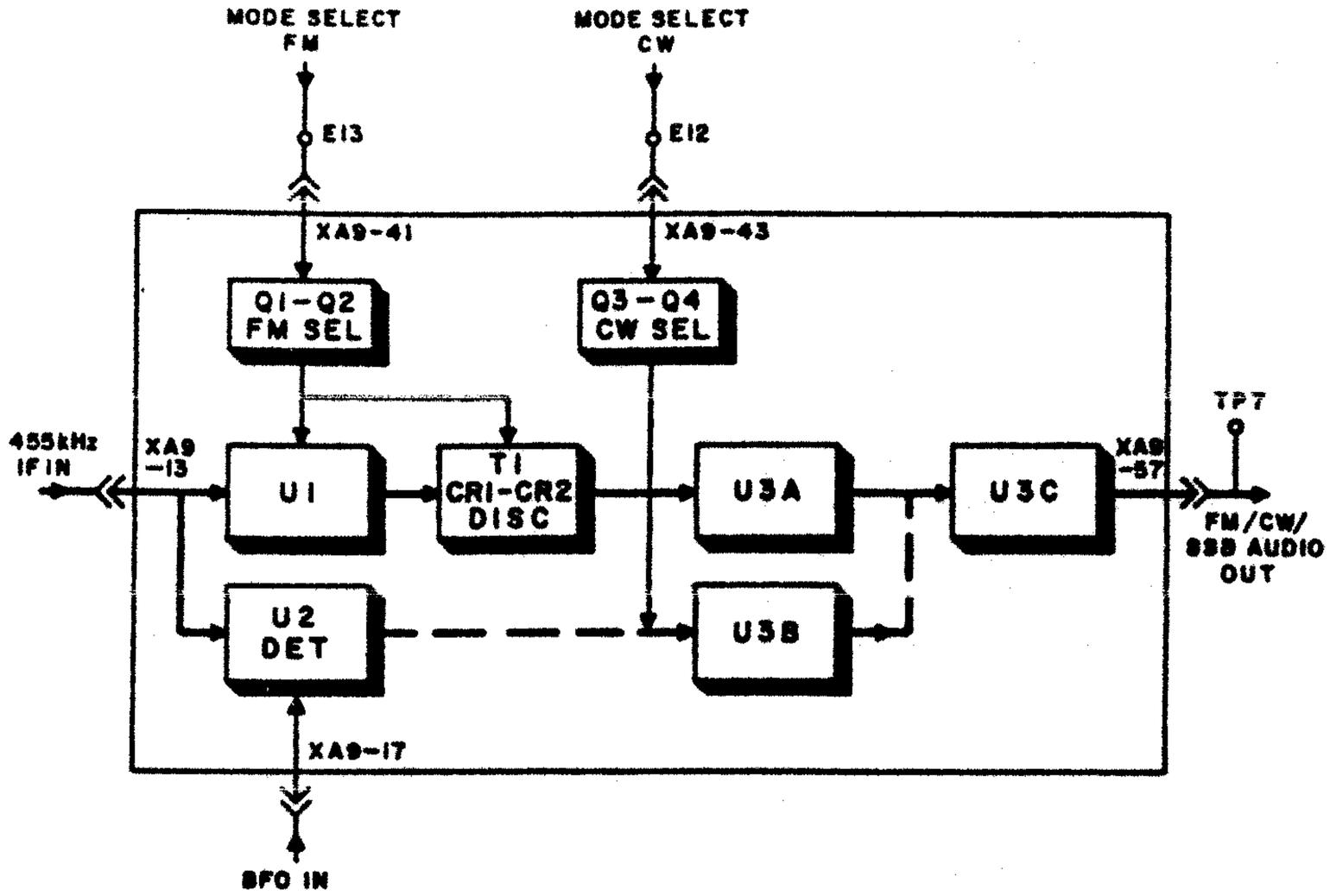


Figure 3-15. FM/CW/SSB Detector Functional Block Diagram.

3.4.12.1 <u>Circuit Description</u>

For FM reception, this module contains a limiter and discriminator. Power for these circuits is supplied when the FM detection mode is selected. For CW or SSB reception, there is a product detector which has its power applied when the CW, USB, LSB, or ISB detection modes are selected. Also, when the product detector is energized, the BFO Synthesizer is enabled and its output is applied to the product detector.

The IF output sample of approximately 10 mV from the 455 kHz amplifier of A4A7 is the input signal for this module. It is applied to both demodulators although only one is actuated at a time. When FM is selected, the control input at pin 41 is high (+5 V) and Q2 and Q1 are turned on. This applies approximately +9 V to limiter U1. The input signal is amplified and clipped by cascaded stages within U1, so its output is free of any amplitude variations. The extent to which the amplitude variations are removed contributes to the AM rejection of the receiver when receiving FM. The output of the limiter drives the Foster-Seeley discriminator. Diodes CR1 and CR2 rectify the composite signals fed to them by C7 and T1. When the signal from the limiter is at exactly 455 kHz, T1 is tuned so that equal and opposite voltages are produced across load resistors R6 and R7, giving a net output of zero to buffer U3A. For inputs slightly off 455 kHz, the voltages of R6 and R7 do not cancel causing a positive output for inputs above 455 kHz and a negative for those below 455 kHz. (Note that these polarities are reversed by U3C, so the output of the module will go negative when the signal frequency increases.) Proper adjustment of L1 will make the output voltage vary linearly with input frequency over ±8 kHz from 455 kHz. At the output of U3A, a low-pass filter, L3 and C11, reduces higher frequency noise components which are present in the discriminator output. When the CW mode or any of the sideband modes is selected, the control input on pin 43 is high (+5 V). This turns on Q4 and Q3, applying +9 V to balanced modulator U2. The BFO is also applied to U2 (approximately a 40 mV level). This allows U2 to act as the 4th mixer in the signal path as described in the Synthesizer Relationships section. Its action may be considered to down-convert IF signals to the audio frequency range. For sideband signals, proper tuning of

the receiver places the center of the IF signal at the frequency corresponding to the carrier frequency of the received signal. This causes the audio components out of U2 to reconstruct those of the original signal transmitted. For CW signals, the BFO is offset from the signal either by use of the BFO offset control on the front panel to cause an audible tone at the audio output when a signal is present.

The output of U2 goes through low-pass filter L2 and C17, which reject higher frequency noise components, to buffer U3B. OP AMP U3C acts as a summing amplifier for the outputs of the FM discriminator or product detector when either is present. It gives different amplifications to these two signals to bring them up to approximately equal levels. The audio output of this module goes to both the Audio Amplifier and the FM Audio terminal of TB2 on the rear of the receiver.

3.4.13 TYPE 746001-1 AUDIO AMPLIFIER (A4A10)

Figure 3-16 is a detailed functional block diagram of the Audio Amplifier which should be referred to in the following circuit description. **Figure 6-13**, Audio Amplifier Schematic Diagram, may be referred to for greater component level detail, if desired.

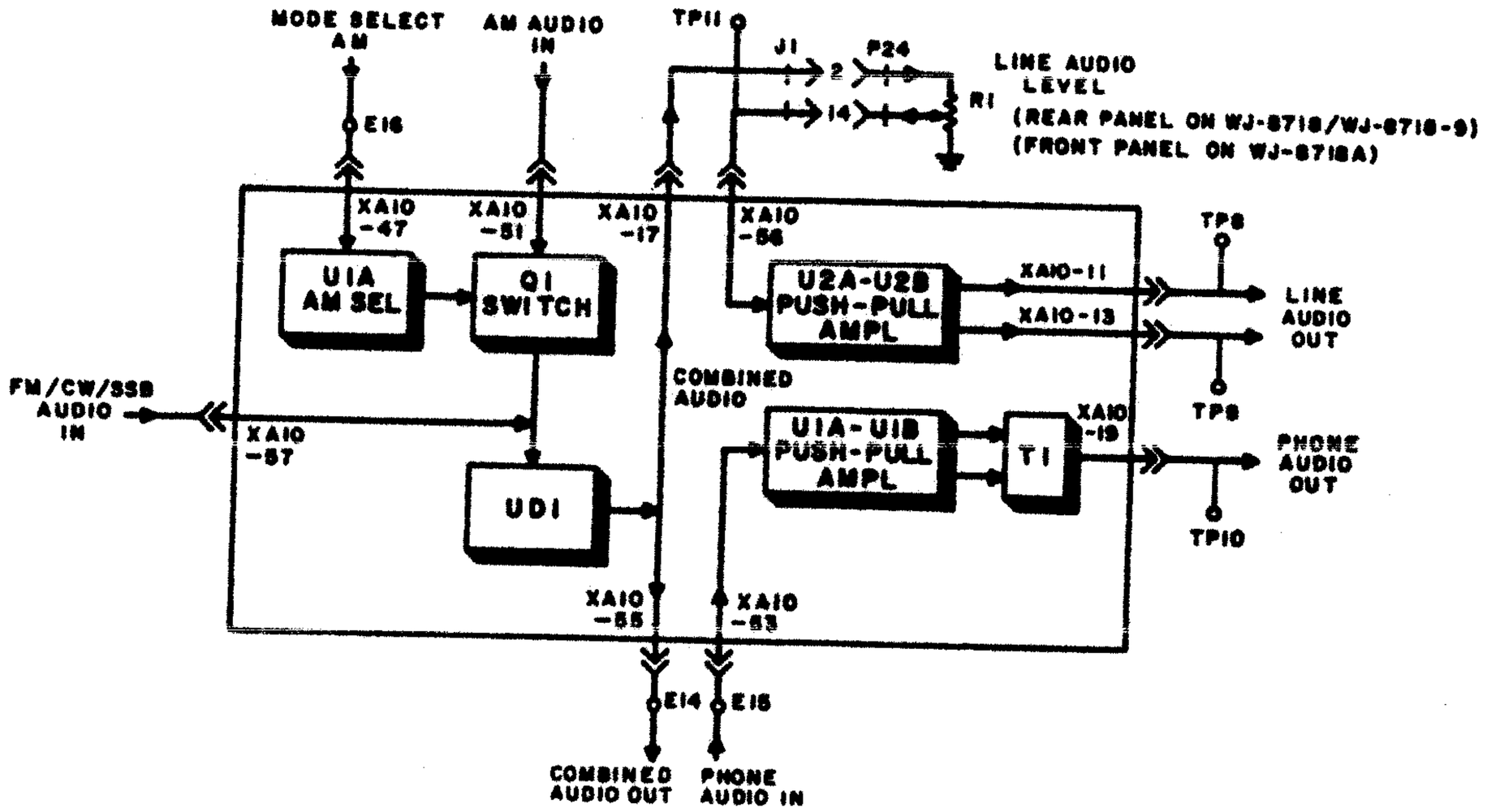


Figure 3-16. Audio Amplifier Functional Block Diagram.

3.4.13.1 Circuit Description

The Audio Amplifier combines the audio outputs of the AM detector and FM/CW/SSB Detector and feeds them to the LINE AUDIO LEVEL control on the rear panel and the PHONE LEVEL control on the front panel. The signal returned from the wiper of the LINE AUDIO LEVEL potentiometer drives the line audio amplifier. The signal returned from the PHONE LEVEL control drives the auxiliary phone amplifier which feeds the PHONE AUDIO terminals on TB1. A rectifier which samples the output of the line audio amplifiers supplies dc to operate the front panel meter in the LINE AUDIO setting.

When the AM detection mode is selected, the control input to pin 47 is high (+5 V). The output of U1A is +14 V, which reverse biases CR1. The gate of FET Q1 will then assume the same potential as its source and Q1 will be on, acting as a closed switch for AM audio. Both demodulators of the FM/CW/SSB Detector will be off so the output of U1D will be AM audio only. When any other detection mode is selected, the control input to pin 47 will be low (0 V) and the output of U1A will be approximately -14 V. This will tend to forward bias CR1 and will cause gate of Q1 to be similarly negative, cutting off all signal flow through Q1. The audio signal from the FM/CW/SSB Detector will appear at the output of U1D.

The signal into line audio amplifier U2 is the output of U1D attenuated by the LINE AUDIO LEVEL control, R1. The two sections of U2 act as a push-pull bridge amplifier, driving output transformer T2 located on the inside of the rear panel. The amplifier U2 uses a supply voltage of +12 Vdc from U4 on the main chassis. Type 746001 is current-limit protected by U4 on the main chassis which provides the +12 Vdc power. A circuit within U2 provides a bias voltage at pin 1 which is equal to one-half the supply voltage. This is connected to the non-inverting inputs of both amplifier sections of U2. Both amplifiers use unity feedback at dc, that is, the only dc path to the inverting inputs is from the outputs, so there is very little dc difference between their outputs at pins 2 and 13.

The input signal is applied to the non-inverting input of U2B, pin 9. Although pins 6 and 9 are at the same dc potential, pin 6 is bypassed so no ac signal appears there. The operation of amplifier U2B will be clear if pin 7, the inverting input of U2A, is considered to be at ac ground. With this assumption, U2B simply appears as a non-inverting amplifier with a closed-loop ac gain of 50. Its ac gain is determined by the ratio of feedback resistors R20 and R19. On the other hand, U2A may then be viewed as an inverting amplifier with an ac gain of nearly one. Its input is the full output of U2B and its gain is determined by R20 and R19 acting as input resistors and R21 as feedback resistor. As with inverting OP AMPs, extremely little signal voltage appears at the amplifier inverting input terminal, thus satisfying the assumption made to explain the behavior of U2B. The net gain of the combined amplifier is 100 and its outputs are balanced with respect to ground. Due to the high current U2 can pass, it is grounded separately from the other circuits on the Audio Amplifier module to prevent ground current coupling which might lead to instability and parasitic oscillations.

The output signal of U2A is rectified and filtered to indicate LINE AUDIO level on the front panel meter. The rectifier is a voltage doubler consisting of CR2, CR3, C12, and C13. It responds to peak-to-peak input voltage and is calibrated by resistors R22, R23, and R24 to indicate the RMS value of a sine-wave at the LINE AUDIO terminals of TB1 on the rear panel. Its calibration is therefore most accurate for sine-wave voltages.

The auxiliary phone amplifier U1B and U1C is a low power bridge amplifier and is therefore similar to U2. It operates from both +15 V and -15 V supplies and has its inputs biased at ground. Comparing its circuit with that of U2 it should be apparent that it also uses unity dc feedback and has a closed loop gain of 100 for ac signals. Its output current capability is much lower than U2, so it can only supply 100 mW compared to 1 Watt from U2.

3.4.14 SYNTHESIZER CIRCUIT DESCRIPTIONS

The following paragraphs provide detailed circuit descriptions for each of the four synthesizers and the time base used in the WJ-8718A HF Receiver. A brief discussion of synthesizer relationships is found in **Paragraph 3.2.2, 3.3.2.2, 3.3.3.2** and **3.3.4.**

3.4.15 GENERAL PHASE LOCK LOOP THEORY

Prior to discussing specific circuit characteristics of the WJ-8718A synthesizer, it is helpful to review the general theory of the circuits used in phase lock loop synthesizer.

3.4.15.1 Basic Phase Lock Loop

The phase lock loop is the method used in this receiver to provide accurate numerical control of the local oscillator frequencies. This technique allows the oscillators to be controlled by any appropriate source of BCD digital data, including remote control sources. The basic phase lock loop is composed of four circuits: a phase detector, a low-pass filter (sometimes called a lead-lag filter, integrator, or loop filter), a voltage-controlled oscillator (VCO), and a frequency divider (counter). A basic phase lock loop configuration is shown in **Figure 3-17.** Depending on the application, the frequency divider circuit may be fixed (to divide by a certain number), or may be programmable to divide by any number in a specific range (20 to 29, for example). The frequency divider may consist of several counters cascaded together, to provide division by a large number. The operation of the basic phase lock loop requires a stable fixed frequency source, to be used as the reference frequency. This receiver contains a temperature-compensated crystal oscillator (TCXO) to provide the basic reference frequency, and may also be operated using an externally supplied 1 MHz reference signal. Both fixed and programmable loops are discussed in the following paragraphs.

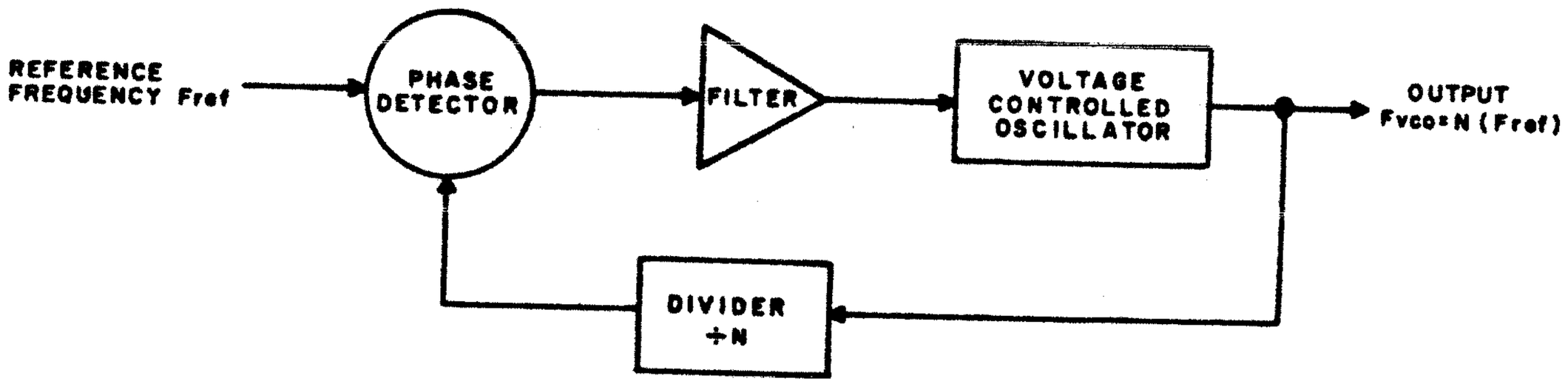


Figure 3-17. Basic Phase Lock Loop Configuration

3.4.15.2 Programmable Phase Lock Loop

The basic phase lock loop technique compares the frequency and phase of an incoming reference signal to the output of the voltage controlled oscillator (VCO). If the two signals differ in frequency and/or phase, an error voltage is generated by the phase detector/filter and applied to the VCO, causing it to correct in the direction required for decreasing the frequency/phase difference. The phase detector produces output pulses which are related to the frequency/phase difference. The filter circuit averages (integrates) these pulses into a proportional error correction voltage. This voltage is applied to control the capacitance of a varicap diode in the VCO circuit, and thus tune the VCO toward the correct

frequency. The correction procedure continues until lock is achieved, after which the VCO will track the incoming reference signal.

Dividing a VCO output by two before applying it to the phase detector results in an error voltage that drives the VCO to twice the reference frequency. A divide-by-3 action results in an error voltage that drives the VCO to three times the reference frequency. Thus, the reference frequency is always multiplied by the divider ratio to give the VCO output frequency. From this, the following relationship can be given:

$$F_{vco} = N\,(F_{ref})$$

An example of the basic phase lock loop technique, using numbers, will provide an understanding of its actual operation. Referring to **Figure 3-18**, the desired frequency is obtained by programming the variable divider through selectable inputs. Assuming the VCO is locked at the desired frequency of 25 MHz, this signal enters the input of the (in this case) divide-by-25 counter (divider). The counter emits a pulse at its output each time 25 pulses enter its input. Therefore, the 25 MHz input results in an output of 1 MHz. This 1 MHz signal is compared to the reference frequency of 1 MHz, indicating a locked situation. If the divider's output had been less than 1 MHz, the phase detector would have produced pulses to drive the VCO to a higher frequency. Similarly, if the divider's output had been greater than 1 MHz, the VCO would have been driven to a lower frequency. An important concept to be noted here is that the phase lock loop's output frequency is dependent upon the selectable inputs of the variable divider.

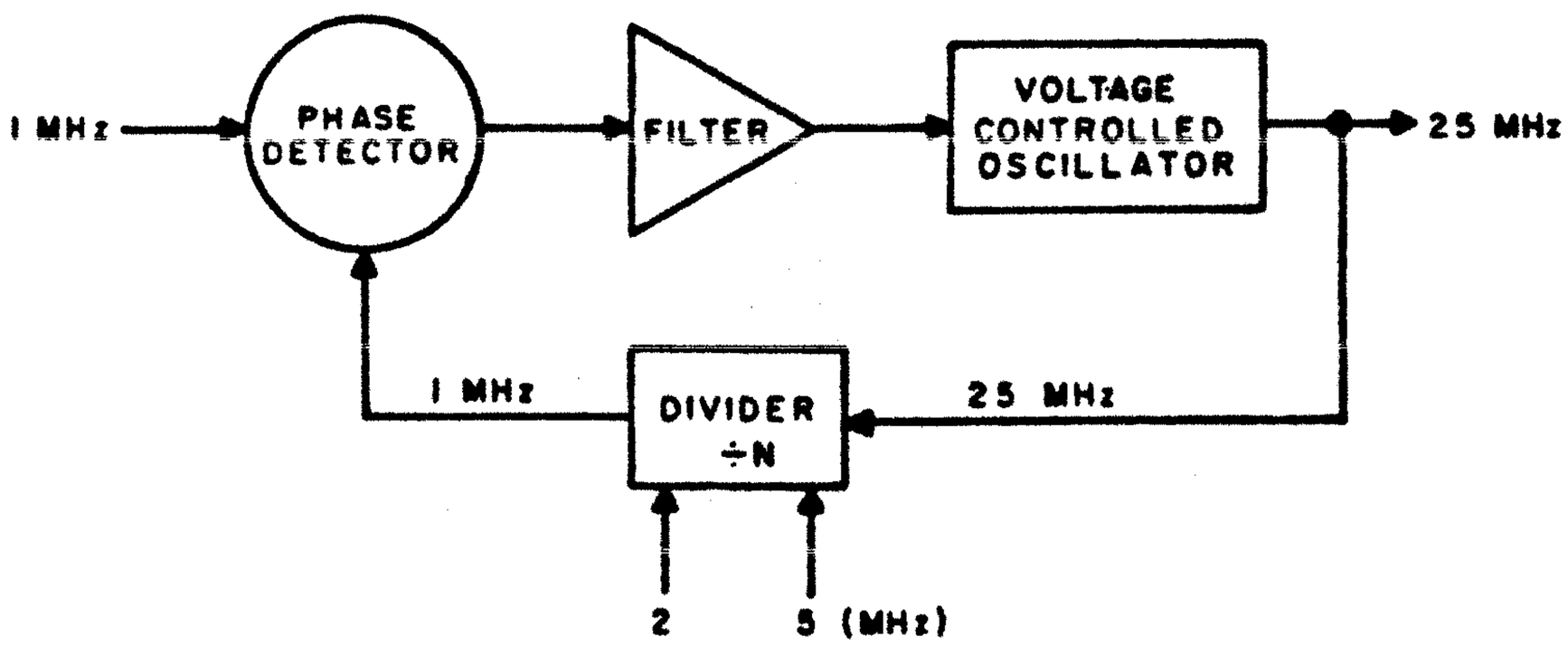


Figure 3-18. Programmable Phase Lock Loop

3.4.15.3 Prescaling Technique

A variation of the basic phase lock loop, shown in **Figure 3-19**, is utilized in the 1st and 2nd LO Synthesizers. The divider portion consists of a two modulus prescaler and two programmable counters. The two-modulus (divider) prescaler accepts the output from the VCO and divides it by one of two numbers (P or P+1). The prescaler in the 1st LO is a divide-by-

50/51 counter and the 2nd LO prescaler is a divide-by-100/101 counter. The swallow counter controls the number of times the prescaler divides by P+1. The programmable counter counts the number of pulses from the prescaler. Totally, these three components provide for coarse (N) and fine (A) tuning of the VCO.

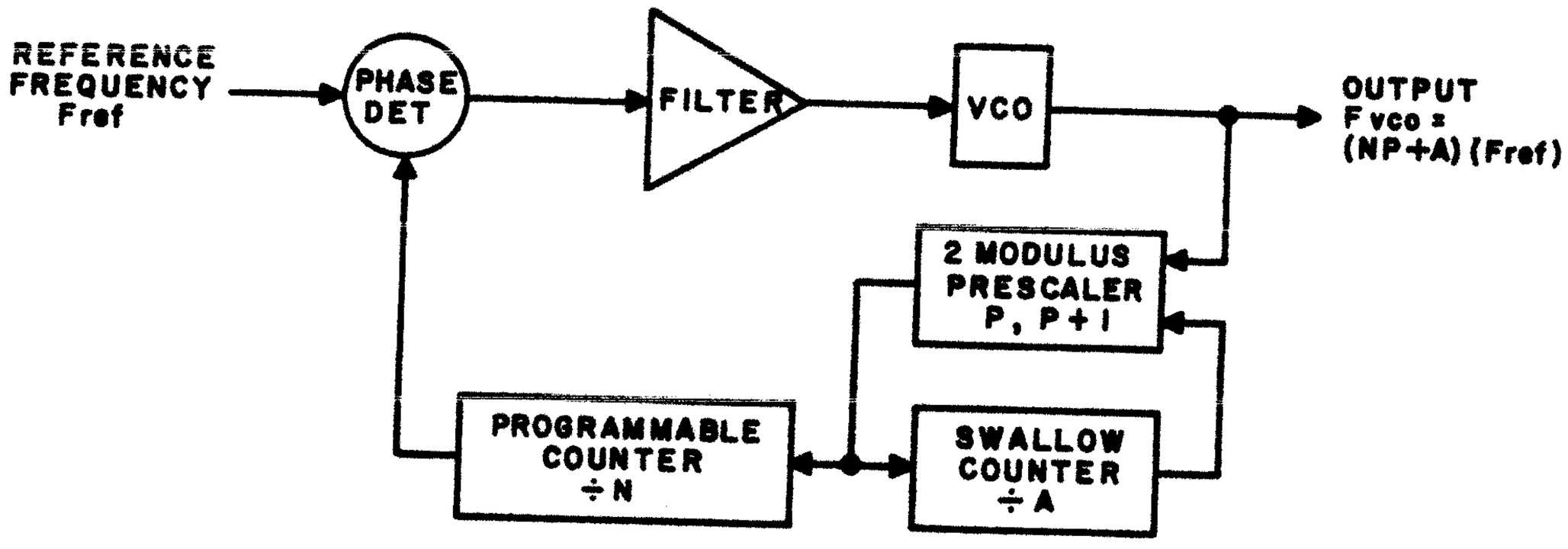


Figure 3-19. Two-Modulus Prescaling in the Phase Lock Loop

In operation, the prescaler divides by P+1, A times. For every P+1 pulse from the prescaler, both the swallow counter and programmable counter are decremented by 1. The prescaler divides by P+1 until the swallow counter reaches its zero state. At this point, the modulus of the prescaler changes to P and the swallow counter is disabled. The prescaler then divides by P until the remaining count in the programmable counter (N-A) decrements to zero. At this time the output of the programmable counter emits a pulse while the swallow and programmable counters are reset. The cycle then repeats.

An example of the two-modulus prescaling technique is given in **Figure 3-20.** For illustration, a VCO output of 153 MHz is desired. Selected into the programmable counter are the two most significant digits, 1 and 5. Selected into the swallow counter is the least significant digit, 3. Under lock conditions, the divider has an input of 153 MHz and an output of 1 MHz.

To produce a 1 MHz signal from a 153 MHz signal requires a divide ratio of 153. The table in **Figure 3-20** shows a count sequence with 153 input pulses resulting in one output pulse. Similarly, a 153 MHz input results in a 1 MHz output. The programmable counter emits

a pulse every time it counts 15 pulses. With the swallow counter set to three, the prescaler divides-by-11 three times and then switches to the divide-by-10 state. At this point, the programmable counter needs 12 input pulses before emitting an output pulse. The prescaler then divides-by-10 twelve times to finish the count sequence. With 3 counts of 11 (3x11=33), and 12 counts of 10 (12x10=120), one output pulse emits from the programmable counter every 153 input pulses (33+120=153).

The two phase lock loop types described are used throughout the WJ-8718A synthesizer section. The 1st LO and part of the 2nd LO utilize the prescaler configuration while the 3rd LO and another part of the 2nd LO use a fixed divide-by-N ratio. The BFO uses the basic phase lock loop configuration, utilizing the divide-by-N technique (F_{VCO}=N F_{ref}). Common to all the synthesizers in this receiver is the phase detector used. It will be described in detail below.

PROGRAM COUNTER	SWALLOW COUNTER	PRESCALER COUNTS	INPUT PULSES
15	3	0	0
14	2	11	11
13	1	11	22
12	0	11	33
11	-	10	43
10	-	10	53
9	-	10	63
8	-	10	73
7	-	10	83
6	-	10	93
5	-	10	103
4	-	10	113
3	-	10	123
2	-	10	133
1	-	10	143
0	-	10	153

153 INPUT PULSES = 1 OUTPUT PULSE

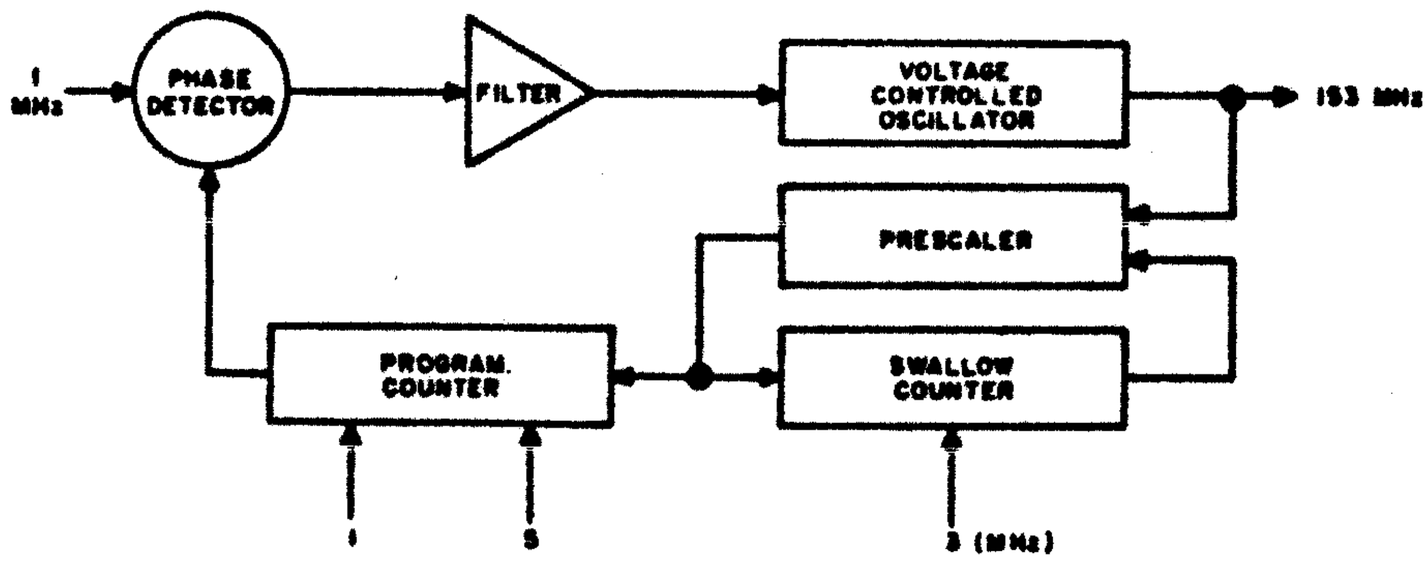


Figure 3-20. Prescaler Dividing Technique

3.4.15.4 Phase Detector

The phase detector used in all of the synthesizers is actually a phase and frequency detector. The integrated circuit also includes a charge pump and an amplifier. Each of these three sections will be discussed below. **Table 3-3** provides some information about the phase detectors in these synthesizers. Refer to the 1st and 3rd LO schematic diagram, **Figure 6-16**, for illustration of typical phase detector operation.

Table 3-3. WJ-8718 Series Phase-Lock Loop Characteristics

Synthesizer	Phase Detector Ref. Des.	Phase Detector Ref. Freq.	Programmable Divider?	VCO Range	Output Frequency
1st LO	U5	40 kHz	YES	171.64-291.60 MHz	42.91-72.90 MHz
2nd LO 32M	U1A,B	1 MHz	NO	32 MHz	
2nd LO PROG	U12A, B	10 MHz	YES	200-210 MHz	
2nd LO OUT	U6A, B	200-210 kHz	NO	32.20-32.21 MHz	32.20-32.21 MHz
3rd LO	U22A, B	5 kHz	NO	11.155 MHz	11.155 MHz
BFO	U9A, B	1 kHz	YES	4461-4639 kHz	446.1-463.9 kHz

The phase detector normally receives a fixed reference frequency at one input (R) and a variable frequency at the input (V) from the divider section. The output responds only to transitions from the two inputs and has four output states as shown in **Figure 3-21.** If the frequency and phase match exactly, outputs U and D remain high. If the variable input leads in phase with respect to the reference input, U remains high and D goes low. If the variable input lags in phase with respect to the reference input, D remains high and U goes low. When inputs V and R are separated by a frequency difference, the output at pins U or D varies high and low at a rate proportional to the difference frequency of the two inputs.

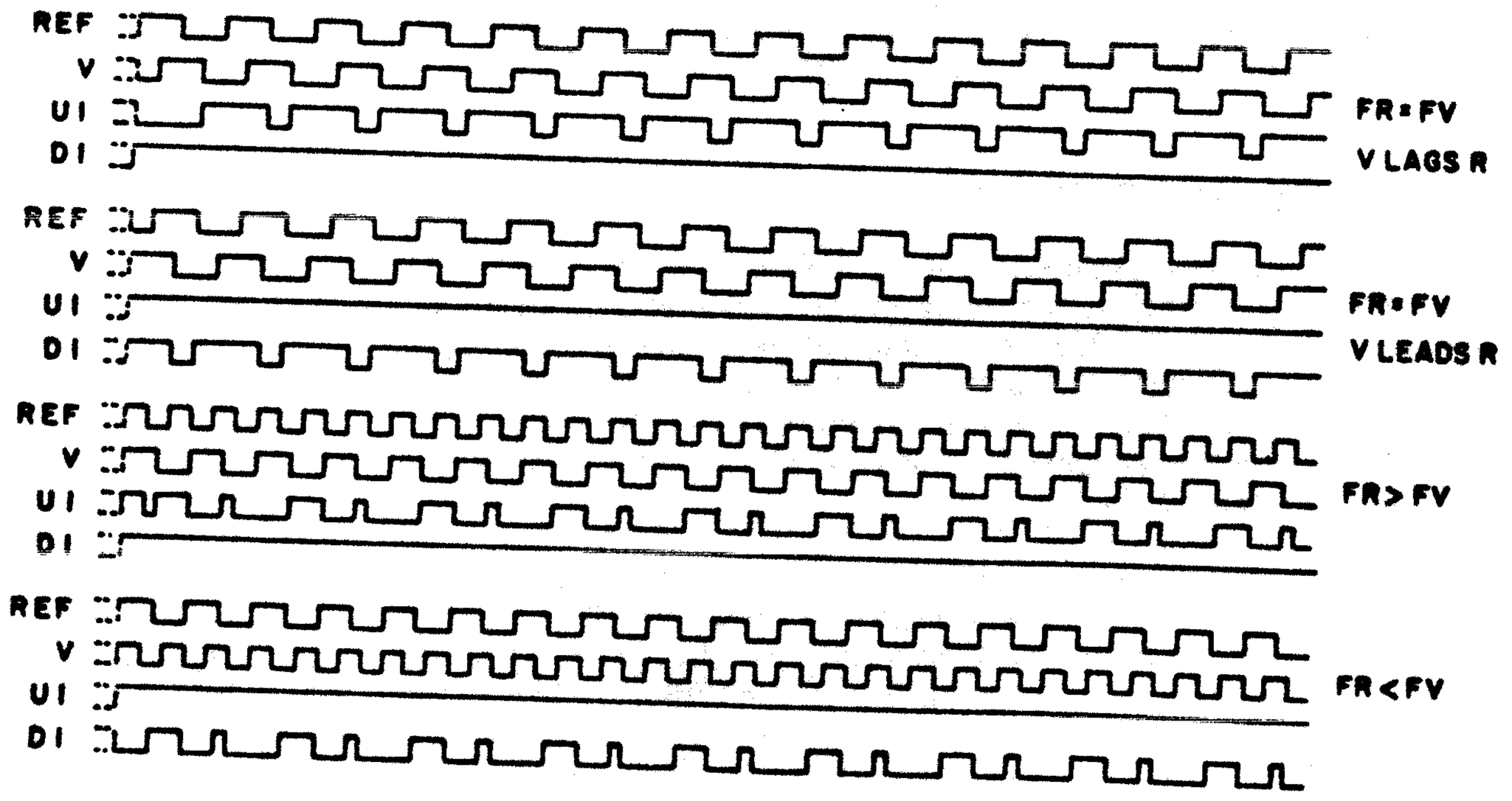


Figure 3-21. Phase Detector Timing Diagram

Under lock conditions, when the input of both V and R are identical in phase and frequency, the output pulses from U and D will be extremely narrow and appear on an oscilloscope as spikes. For a large difference between the two input frequencies, as when a new

LO frequency is established, the outputs respond as described above with wide pulses appearing on the proper outputs.

The charge pump accepts both outputs from the phase detector and translates the voltage levels before they are applied to the loop filter. The input to pin 11 appears as an inverted output at pin 10. The input to pin 4 appears as an output at pin 5. There will be a pulsed waveform entering either pin 4 or pin 11 at any given time. The charge pump delivers voltage commands from 2.25 V on positive swings to 0.75 V on negative swings, with a mean value of 1.5 V. The charge pump outputs are applied to a low-pass active filter.

The active filter normally uses the amplifier contained in the phase detector IC plus external resistors and capacitors. In some cases an external transistor will also be used, or an external OP AMP. This filter has a direct influence on loop bandwidth, capture range, and transient response. Its output is the VCO tuning voltage, which is applied to control the capacitance of a varicap tuning diode in the VCO tank circuit, thereby controlling the VCO frequency.

3.4.16 TYPE 791600-1 1ST LO SYNTHESIZER (A5A1A2)

The 1st LO Frequency Synthesizer circuits are part of the 1st and 3rd LO/Time Base circuit board. The 1st LO utilizes a phase lock loop configuration with the prescaling technique previously described in **paragraph 3.4.15.3.** The output of the 1st LO tunes in 10 kHz steps from 42.91 MHz to 72.90 MHz. This tuning range mixes with the 0.0 to 29.99 MHz receiver tuning range to produce a 1st IF signal in the range of 42.90 to 42.91 MHz. A block diagram of the 1st LO is shown in **Figure 3-22.**

3.4.16.1 Functional Description

The programmable divider, phase detector, and lead-lag filter of the 1st LO Synthesizer are contained on the main circuit board (Type 791600); the VCO and tuning voltage control circuits (Type 791629) are mounted separately, but together with the main circuit board, they form a combined assembly. The phase detector (U5), charge pump (U6C), and lead-lag filter (U7) of the 1st LO will be discussed lightly since a detailed description of these circuits can be found in **paragraph 3.4.15.4** of the phase lock loop section. Refer to **Figure 3-22** for the following discussion.

A two-modulus prescaler (described in **paragraph 3.4.15.3**) is used at the input to the divide-by-N counter to divide down the frequency from the VCO so that it can be handled by conventional low-power Schottky counters. If the 1st LO is locked on the correct frequency, the output of the programmable counter will be 40 kHz. This 40 kHz is compared to the 40 kHz reference frequency from the Time Base in phase detector U5. The difference in frequency and phase of these two input signals produces a series of pulses which the charge pump converts to positive or negative going voltages. These voltages are integrated by lead-lag filter U7 toprovide the tuning voltage for the VCO. The Notch Filter and Tuning Voltage ground reference circuits isolate the VCO tuning voltage from any ripple from the 40 kHz reference frequency. An octal band-switching code, generated by octal encoder U13 from the divider section, switches the VCO to one of eight tuning ranges spaced 16 MHz apart.

The VCO has two inputs and two outputs. The inputs to the VCO are a tuning voltage and a band-switching code. Together they supply the VCO with the necessary

information for tuning to the correct frequency. The actual VCO generates frequencies between 171.64 MHz and 291.60 MHz. This range is sent to the programmable divider of the phase lock loop. The other output of the VCO is applied to a frequency divider. Since the 1st LO frequency range is from 42.91 MHz to 72.90 MHz, the VCO frequency range must be divided by 4. For this same reason, the eight tuning ranges of the VCO (from the band switching code) are spaced 16 MHz apart within the VCO and 4 MHz apart (16 MHz ÷ 4) for the 1st LO output. In summary, the VCO frequency is four times that of the 1st LO output frequency.

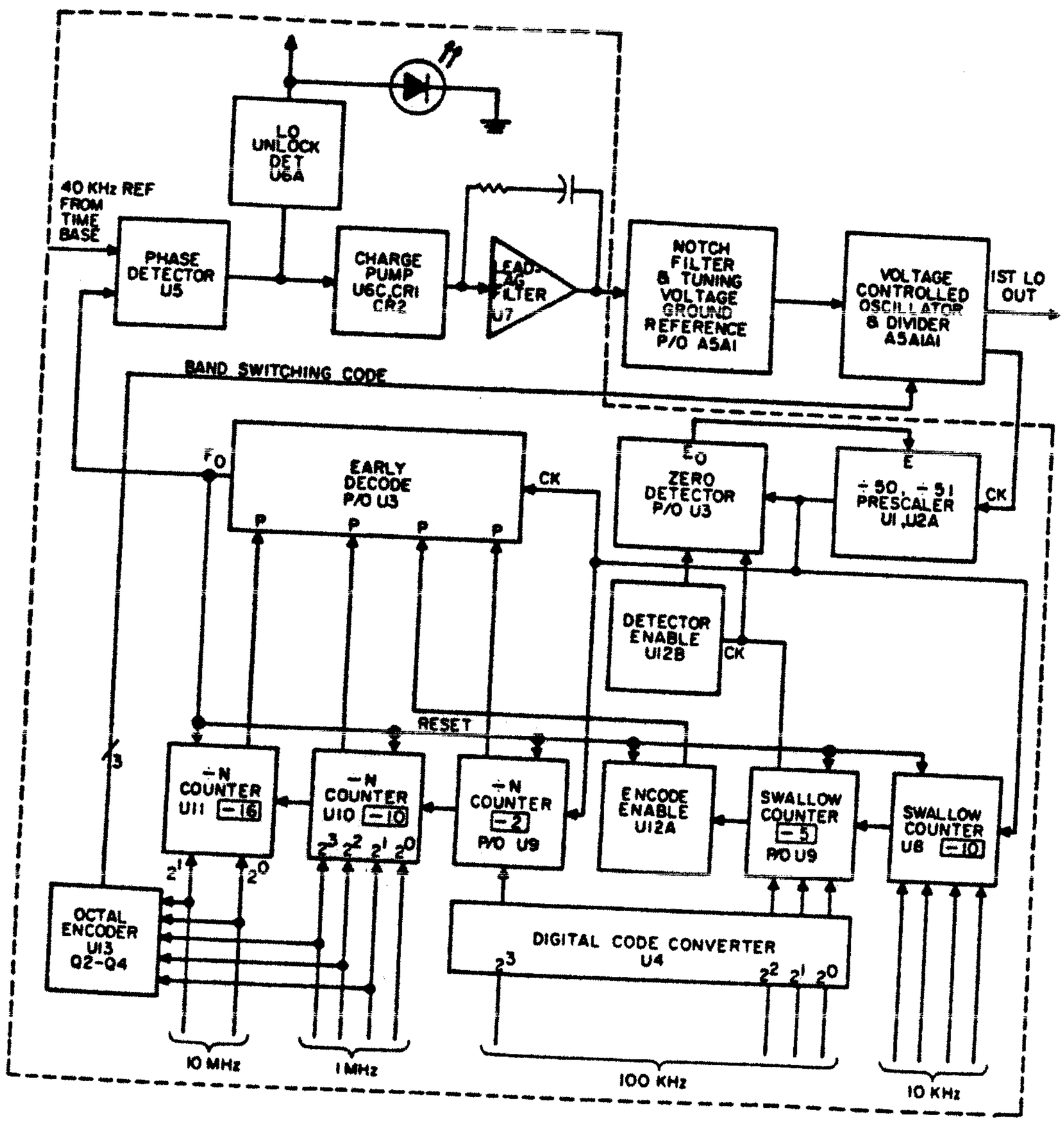


Figure 3-22. 1st LO Functional Block Diagram

The programmable divider has an input range from 171.64 MHz to 291.60 MHz, in 40 kHz steps, and must divide each of these frequencies down to exactly 40 kHz. This condition calls for the programmable divider to have a divide ratio from 4291 (171.64 ÷ 40 kHz) to 7290 (291.60 MHz ÷ 40 kHz).

From the conditions above, the counters within the programmable divider, U8, U9, U10 and U11, must have a divide range from 4291 to 7290. The inputs of the counters are always preset from the BCD equivalents of the four most significant digits of the tuned frequency. This range is from 0000 to 2999. One other condition exists at the input to the counters; U11 is wired to automatically add 8 to its preset. Therefore, the VCO presets have a range from 8000 to 10999. The external logic circuits connected to the counters stop the counters from counting when they reach the terminal count number 3709. Since the counters are wired to count down, the overall divide range needed from the counters is obtained; the divide range is from 4291 (8000-3709) to 7290 (10999-3709).

3.4.16.2 Circuit Description

3.4.16.2.1 Counting Cycle

Although the counters have the correct divide range needed to divide the input frequency down to 40 kHz, the VCO output frequency is too high for the counters to operate properly. Therefore, a high-speed, two-modulus prescaler is used to divide the input frequency to a range that can be handled by the counters.

The prescaler used in the 1st LO divides either by 50 or 51. In order for the counters to divide correctly, they must divide in increments of 50 or 51 also. When the prescaler divides by either 50 or 51, only one pulse is sent to the counters. Therefore, the counters must interpret this pulse as representing either 50 input pulses or 51 input pulses.

The counter section shown in Figure 3-16 is divided into two parts: a programmable counter and a swallow counter. The programmable counter consists of U11, U10, and part of U9, and the swallow counter consists of U8 and part of U9. Both counters receive the same clock pulse from the prescaler output. By having the swallow counter control the prescaler, the represented count will decrement by 51 when the programmable counter and the swallow counter are counting. When the swallow counter reaches terminal count, the prescaler will begin to divide by 50 and the swallow counter will be disabled for the remainder of the cycle.

Figure 3-23 shows graphically a typical 1st LO counting cycle. The prescaler divides by 51 until the swallow counter reaches terminal count. When the outputs of the swallow counter reach this state, they cause the zero detector's E_0 output state to become high. This causes the prescaler to divide by 50 until the end of the count cycle. Since the programmble counter is separately clocked, it continues to count down until its terminal count is detected by the early decode circuit. When this occurs, the $\overline{F_0}$ output of the early decode goes high after the next clock pulse from the prescaler. This is the output pulse supplied to the phase detector. When the output from the early decode circuit again goes low, it resets the counters to the preset number on their inputs. It also causes the reset enable circuit to reset the zero detector circuit causing its output to go low so the prescaler can divide by 51 during the next count cycle.

FIGURE 3-23
FIGURE 3-24

Refer to the schematic diagram of the 1st LO, **Figure 6-17**, to aid in understanding the circuit descriptions presented below.

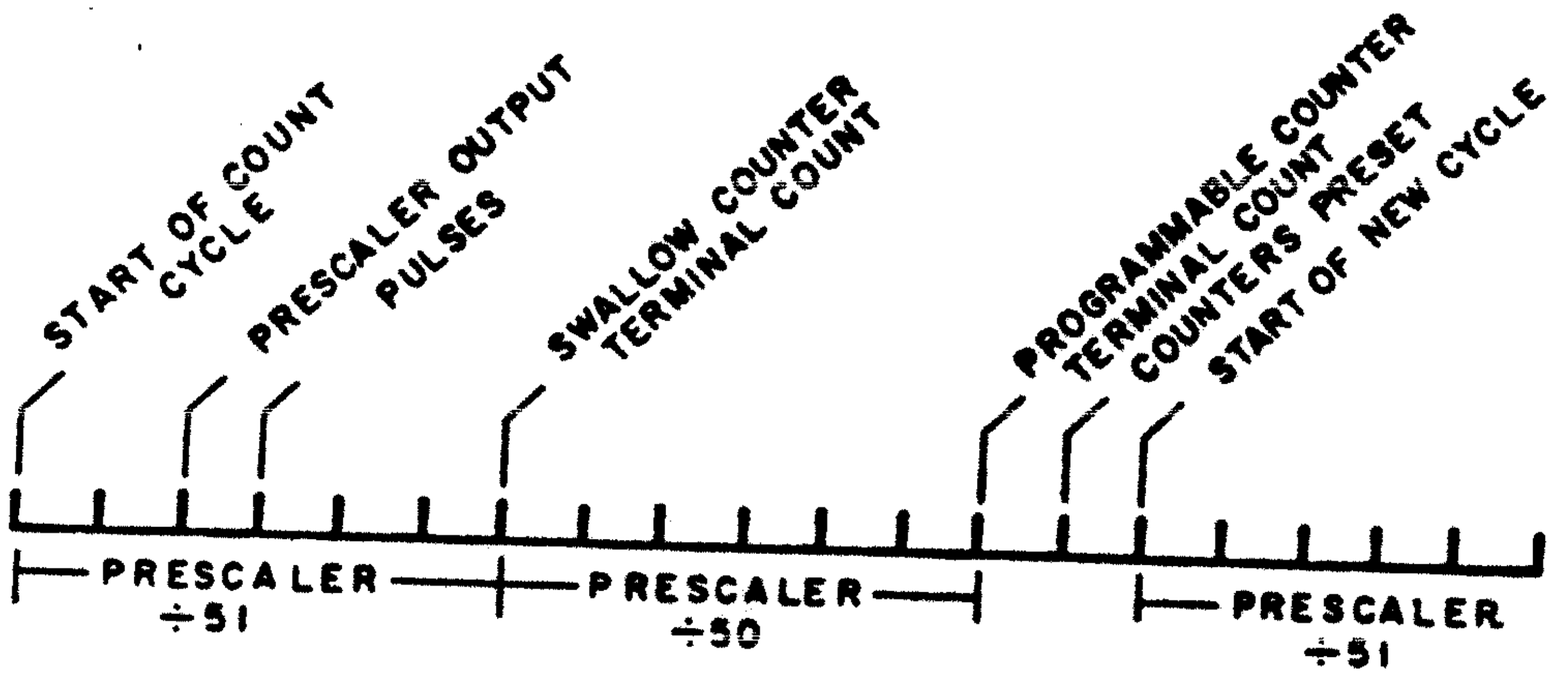


Figure 3-23. 1st LO Counting Cycle

3.4.16.2.2 Prescaler, U1 and U2A

The prescaler input frequency ranges from 171.64 MHz to 291.60 MHz. The prescaler divides this by 50 or 51, depending on the states of the E inputs of U1. **Figure 3-24** illustrates the prescaler's operation. U1 is a divide-by-10/11 counter and U2A is a divide-by-5 counter. The prescaler divides by 51 when E4 is low and when E5 pulses low once for every five pulses from U2A. E5 is low for only one count out of five so the complete count cycle of U1 and U2A takes 51 counts (4 x 10 + 1 x 11). This count cycle continues until the swallow counter reaches terminal count. E4 then goes high and U1 divides by 10 only, giving U1 and U2A a complete count cycle of 50.

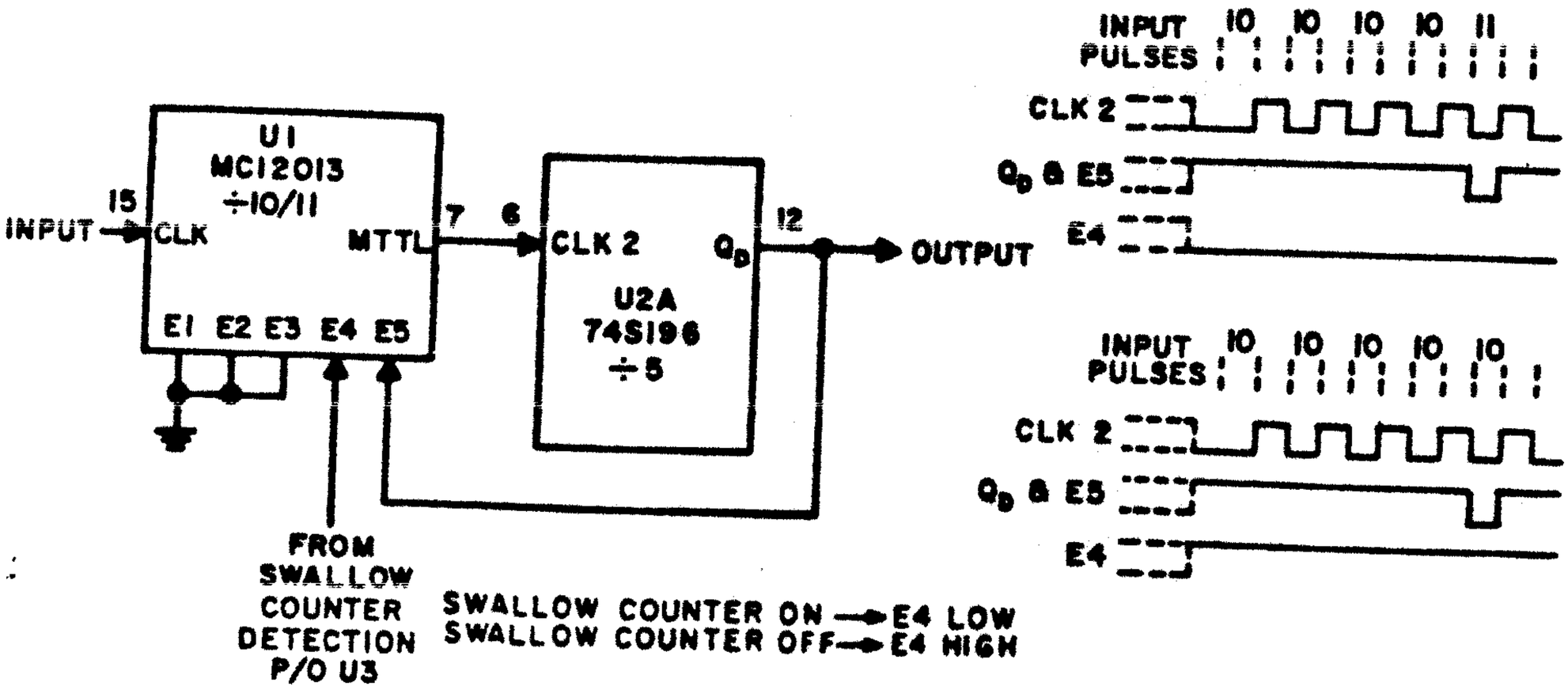


Figure 3-24. 1st LO Prescaler Timing Diagram

3.4.16.2.3 Digital Code Converter U4

U4 is a programmable ROM (Read Only Memory) that serves as a decoder or code converter. It behaves as a look-up table to translate a BCD input, which has bit values of 2^3, 2^2, 2^1, 2^0, to a new code with bit values of 5^1, 2^2, 2^1, 2^0. **Table 3-4** illustrates all possible inputs and outputs of U4.

Table 3-4. Code Converter U4, Truth Table

BCD INPUTS TO U4				OUTPUTS FROM U4			
2^3	2^2	2^1	2^0	5^1	2^2	2^1	2^0
D	C	B	A	Y_4	Y_3	Y_2	Y_1
0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	0	0	1
0	1	0	1	1	0	0	0
0	1	1	0	1	1	0	0
0	1	1	1	1	0	1	1
1	0	0	0	1	0	1	0
1	0	0	1	1	0	0	1

U4 serves as part of the programmable counter and part of the swallow counter. Output Y_4 presets the divide-by-2 counter, which is part of the programmable counter. Outputs Y_1, Y_2, and Y_3 preset the divide-by-5 counter which is part of the swallow counter. The function of U4 in each counter section will be discussed below.

3.4.16.2.4 Programmable Counter U9, U10, U11

The programmable counter is formed by U11, U10, and part of U9. U11 and U10 count down and U9 counts up. U10 is a divide-by-10 counter (BCD). U11 is a divide-by-10 counter (BCD). With the D input of U11 tied high (to Vcc 3), the counter is always preset with at least 8 (1000). The divide-by-2 counter within bi-quinary counter U9 is part of the programmable counter, using preset input A and output QA.

U11, U10, and U9 are cascaded with a clock input entering U9 at pin 8 (CLK1). U9 cascades to U10 and clocks U10 on its the 0 to 1 transition. U10 cascades to U11. The programmable counter counts from its preset values on U11, U10, and U9 down to a detection number of 370 (0011, 0111, 0000). A carry condition is the only exception to this count sequence and will be discussed later.

3.4.16.2.5 Swallow Counter U8, U9

The 1st LO swallow counter is formed by decade counter U8 and the divide-by-5 part of bi-quinary counter U9. Cascaded, they form a divide-by-50 counter which controls the

divide mode of prescaler U1. The counting mode of the swallow counter is unusual, in that U8 counts down and clocks U9, which counts up. Refer to **Table 3-5.** The terminal count for the swallow counter occurs at 09. At this point the Z inputs of control device U3 must all be low. However, the $\overline{Z_0}$ input is controlled by U12B, which enables detection of the terminal count. The Q output of U12B is set high at the beginning of each count cycle, and will not go low until the most significant swallow counter digit, from U9, steps from 1 to 2. This clocks U12B, validates the terminal count, and the prescaler mode will be changed when the counter reaches 09. Therefore, for preset values between 29 and 40, the counter cycles past the first 09 count to the 10 to 29 transition, then terminates at 09.

3.4.16.2.6 Carry Condition U12A, U6B

A carry condition occurs in the programmable counter when the preset to the swallow counter falls into the range of 29 to 00. Refer to **Table 3-5.**

Table 3-5. Count Sequence, 1st LO Swallow Counter

+5 U9B (UP)	+10 U8 (DOWN)	COMMENTS	+5 U9B (UP)	+10 U8 (DOWN)	COMMENTS
0	0	THIS TRANSITION SETS CARRY CONDITION (U8 clocks U9)	3	4	
1	9		3	3	
1	8		3	2	
1	7		3	1	
1	6		3	0	
1	5		4	9	U8 clocks U9
1	4		4	8	
1	3		4	7	
1	2		4	6	
1	1		4	5	
1	0	SWALLOW COUNTER VALIDATE (U8 clocks U9)	4	4	
2	9		4	3	
2	8		4	2	
2	7		4	1	
2	6		4	0	
2	5		0	9	TERMINAL COUNT (U8 clocks U9)
2	4		0	8	
2	3		0	7	
2	2		0	6	
2	1		0	5	
2	0		0	4	
3	9	U8 clocks U9	0	3	
3	8		0	2	
3	7		0	1	
3	6		0	0	
3	5		0	9	Repeat Cycle U8 clocks U9

If the preset to the swallow counter is 00, the first count will cause the transition to 19. When this occurs, the U9 output Q_B will go high, while Q_C remains low. The logic of U24B and U24A produces a logic high to clock U12A. The Q output of U12A is preset high at the beginning of each cycle, but if the 00 to 19 transition occurs, it is clocked low. This applies a logic low to NAND gate U6B, and effectively shifts the actual terminal count of the programmable counter from 370 to 371. (The actual number detected is 380 or 381, for reasons explained later, in **paragraph 3.4.16.2.8**).

3.4.16.2.7 Count Sequence

Table 3-6 illustrates the count-down sequence of the 1st LO divider for two example RF input frequencies. In the first example, the receiver is tuned to 00.00XXX MHz and the 1st LO counter presets are loaded with the value 8000, as explained in **paragraph 3.4.16.1.** The two most significant preset digits (8 and 0) are loaded directly into U11 and U10. The least significant digit (0) is loaded directly into U8. The 0 applied to code converter U4 results in a 0 preset to both sections of U9, as explained in **paragraph 3.4.16.2.3.** The swallow counter (U8, U9B) and the programmable counter (U9A, U10 and U11) are both decremented by 1 prescaler output pulse for each 51 prescaler input pulses. When the swallow counter reaches its terminal count (at 09) the prescaler divide mode changes to 50. Since the swallow counter was preset with 00, a carry condition exists and the terminal count for the programmable counter is 371, as explained in **paragraph 3.4.16.2.6.** When the programmable counter reaches terminal count, the cumulative number of pulses into the prescaler equals 4291. Since the loop reference frequency is 40 kHz, the VCO frequency is 4291 x 40 kHz, or 171.64 MHz. The VCO output to the mixer is divided by 4, resulting in an actual LO output of 42.91 MHz. This is the LO frequency corresponding to a tuned RF of 00.00XXX MHz.

The second example in **Table 3-6** shows the receiver tuned to 29.99XXX MHz and the 1st LO counter presets loaded with the value 10999. The two most significant preset digits (10 and 9) are loaded directly into U11 and U10. The least significant digit (9) is loaded directly into U8. The 9 applied to code converter U4 results in a value of 1 applied to U9A, and a value of 1 applied to U9B, as explained in **paragraph 3.4.16.2.3.** Since the swallow counter preset is 19, no carry condition exists and the terminal count for the programmable counter is 370. When terminal count is reached, the cumulative number of pulses into the prescaler equals 7290. With a loop reference of 40 kHz, the VCO frequency is 291.6 MHz, and the actual LO output (291.6 MHz ÷ 4) equals 72.90 MHz. This corresponds to a tuned RF of 29.99XXX MHz.

Table 3-6. 1st LO Divider Count-Down Cycles

Pre-Scaler Mode	Pulses into Prescaler New	Pulses into Prescaler Cum.	Prescaler Output Pulses	U9B (÷5)	U8 (÷10)	U11 (÷16)	U10 (÷10)	U9A (÷2)	COMMENTS
÷51	0	0	0	0	0	8	0	0	Preset for Tuned Freq. of 00.00XXX MHz
	51	51	1	1	9	7	9	1	
	51	102	1	1	8	7	9	0	
	408	510	8	1	0	7	5	0	
	51	561	1	2	9	7	4	1	Swallow Ctr. Validation
	1530	2091	30	0	9	5	9	1	Swallow Ctr. Terminal Count
÷50	50	2141	1			5	9	0	
	900	3041	18			5	0	0	
	1000	4041	20			4	0	0	
	100	4141	2			3	9	0	
	50	4191	1			3	8	1	Early Decode Terminal Count (Carry Condition) Divide Ratio = 4291
	100	4291	2			3	7	1	
	4291 x 40 kHz = 171.64 MHz								
÷51	0	0	0	1	9	10	9	1	Preset for Tuned Freq. of 29.99XXX MHz
	51	51	1	1	8	10	9	0	
	408	459	8	1	0	10	5	0	
	51	510	1	2	9	10	4	1	Swallow Ctr. Validation
	1530	2040	30	0	9	8	9	1	Swallow Ctr. Terminal Count
÷50	1000	3040	20			7	9	1	
	1000	4040	20			6	9	1	
	1000	5040	20			5	9	1	
	1000	6040	20			4	9	1	
	1000	7040	20			3	9	1	
	150	7190	3			3	8	0	Early Decode Terminal Count (No Carry Condition) Divide Ratio = 7290
	100	7290	2			3	7	0	
	7290 x 40 kHz = 291.60 MHz								

3.4.16.2.8 Divider Section Terminal Count

The terminal counts of both the swallow counter and the programmable counter are detected by the terminal count control IC, U3. The prescaler mode is controlled by the swallow counter logic outputs applied to the Z inputs of U3, as described in **paragraph 3.4.16.2.5.** The terminal count of the programmable (main) counter is obtained when the correct logic levels are applied to the P and B inputs of U3. As previously stated, the actual terminal count occurs at 370 (or 371, with the carry condition). However, because of the relatively high counting speed, the counters require about two clock pulses to reset at the end of each counting cycle. Therefore, the divider makes use of a two-pulse "early decode" circuit contained in U3, **Figure 3-25.**

When the terminal count logic conditions are satisfied (at the P and B inputs) U3 counts one clock pulse, then drops the F_0 output line low. This resets the flip-flops and presets (loads) the counters. At the end of the second clock pulse, the F_0 output goes high, starting the count cycle and clocking the VCO phase detector, U5. Therefore, the number detected by U3 is 380 (or 381, in the carry condition) but the actual terminal count is 370 (or 371), because two more prescaler output pulses occur before the F_0 output goes high.

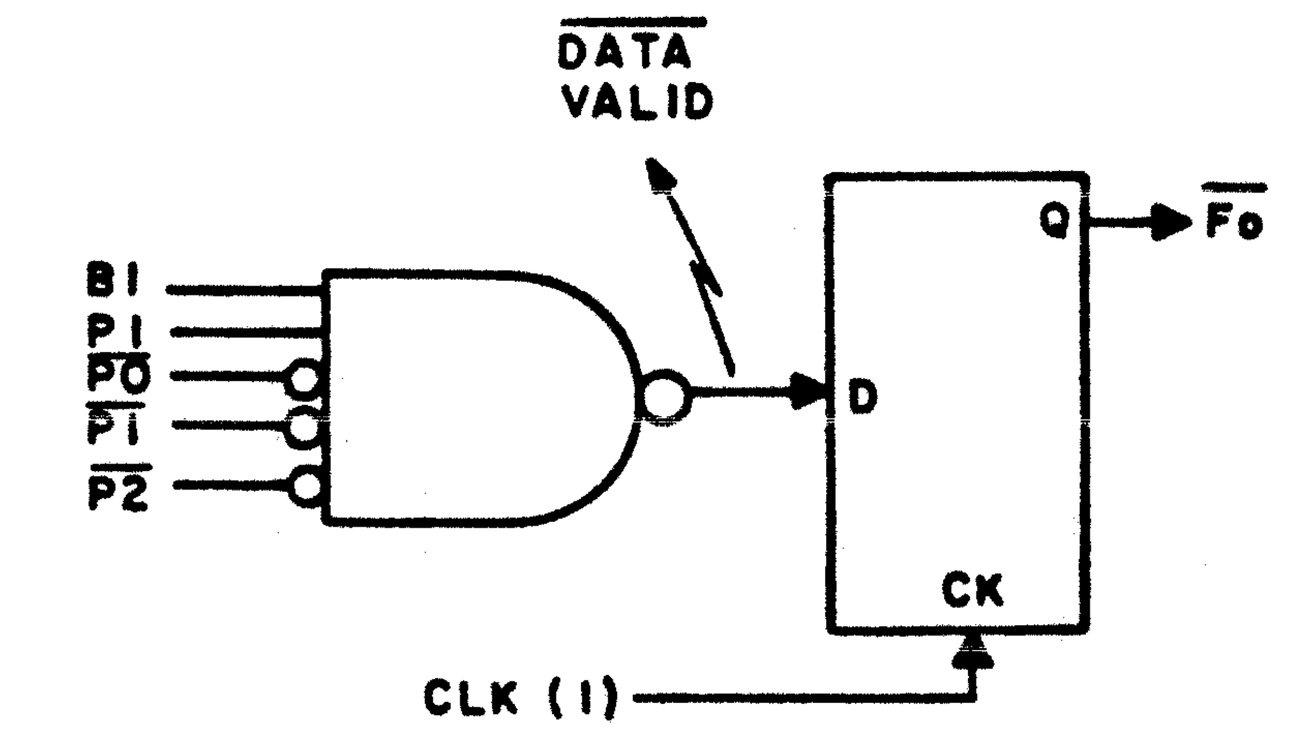


Figure 3-25. Two-Pulse Early Decode, Count Termination

3.4.16.2.9 VCO Band Select Code

The VCO Band Select circuits are shown in the 1st and 3rd LO Synthesizer schematic diagram, **Figure 6-17**. The purpose of U13, Q2, Q3, and Q4 is to translate the 1st LO frequency range into eight different bands for the VCO. The band select code causes different combinations of inductance to be placed across the VCO tuning circuitry, thereby changing the VCO frequency range.

Octal encoder U13 accepts BCD inputs from the two most significant digits of the 1st LO frequency word and translates them into a binary coded word on Y_2, Y_3, and Y_4. The transistors connected to these outputs supply negative true-code outputs. For example, when Y_2 is low, -12 V appears at the base and emitter of Q2 turning the transistor off. This causes the collector to be off and +15 V to appear at output E1. When Y_2 is high, Zener diode CR8 conducts causing Q2 to turn on, resulting in a -12 V potential at output E1. The relationship of the band select code to the LO frequency word is detailed in **Table 3-7.**

Table 3-7. Band Select Coding

RF Digit		Band Select Code (Negative True)		
10 MHz (U11)	1 MHz (U10)	2^2 (E3)	2^1 (E2)	2^0 (E1)
0	0	0	0	0
0	4	0	0	1
0	8	0	1	0
1	2	0	1	1
1	6	1	0	0
2	0	1	0	1
2	4	1	1	0
2	8	1	1	1

3.4.17 TYPE 791629 VOLTAGE CONTROLLED OSCILLATOR (A5A1A1)

3.4.17.1 Functional Description

Figure 3-26 is the functional block diagram for the Voltage Controlled Oscillator. The VCO is an integral part of the 1st LO Synthesizer loop, whose inputs are a tuning voltage and a band select code, and whose output is the 1st LO frequency. The VCO operates at a frequency four times the desired 1st LO frequency. The band select code and the tuning voltage combine to tune the oscillator from 171.64 MHz to 291.60 MHz in 40 kHz steps. The oscillator output is amplified by Q2 and split between the buffer amplifier and the Divide-by-4 Assembly. Buffer amplifier Q3 provides the synthesizer with a sample of the oscillator signal. The sample is processed and, if required, a correction is made to the tuning voltage. The amplified oscillator frequency is divided by 4 (by U1) since the oscillator frequency is actually four times the desired 1st LO frequency. Amplifier Q7 supplies a high-level signal for the 1st Mixer. A further explanation of the VCO follows.

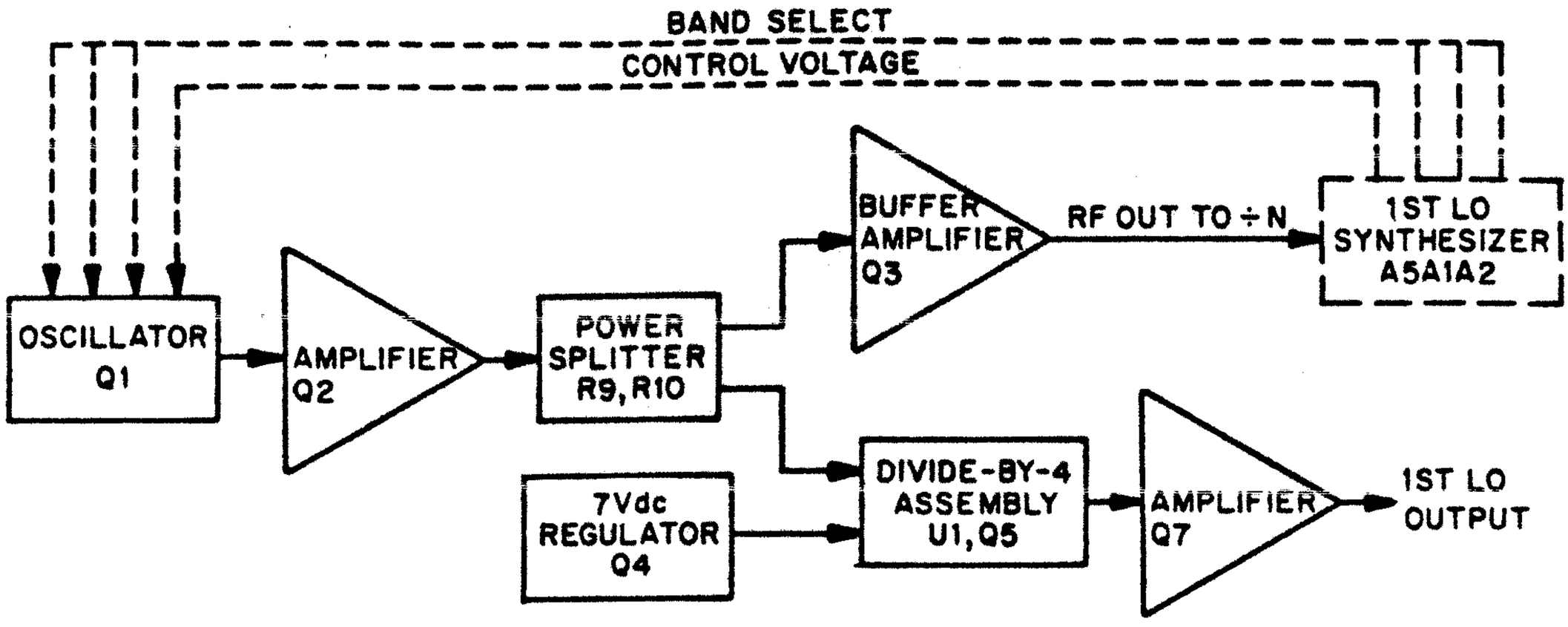


Figure 3-26. VCO Functional Block Diagram

3.4.17.2 **Circuit Description**

Refer to **Figure 6-16** for the schematic diagram of this circuit. This description follows the same organization as the functional description given in the preceding paragraph.

Applying a negative-true-code voltage to the BAND SELECT inputs tunes the oscillator to one of eight different frequency bands. When the BAND SELECT inputs are all positive, CR1 through CR3 are off, and L2 through L4 are effectively out of the circuit. This allows the inductance of T1 to be maximum. When any or all of the BAND SELECT inputs are negative, the corresponding diode will conduct and the inductance of T1 will be reduced by the shunting effect of the inductor (L2, L3, or L4). Varactor diode CR4 fine tunes the oscillator in response to the tuning voltage input. Common-emitter amplifier Q2 keeps load changes at the input of power divider R9 and R10 from being reflected back to the output of oscillator Q1. T2 matches the output of the amplifier to the input of the power divider. The signal is coupled to buffer amplifier Q3, which drives the prescaler of the synthesizer. R9 and C15 couple the signal from Q2 to the input of the divide-by-4 circuit U1. MECL divider U1 divides the signal frequency by four and amplifier Q5 isolates its output from load changes. Voltage regulator Q4 provides U1 and Q5 with a -7.0 V power input from the -12 V power supply input to the assembly. Amplifiers Q5 and Q7 provide the relatively high currents needed to drive the input of the 1st Mixer.

3.4.18 TYPE 791601 2ND LO SYNTHESIZER (A5A2)

3.4.18.1 Functional Description

The 2nd LO tunes from 32.20001 to 32.21000 MHz in 10 Hz steps. This synthesizer utilizes three phase lock loops to produce the 2nd LO output. The functional block diagram of the 2nd LO is shown in **Figure 3-27.**

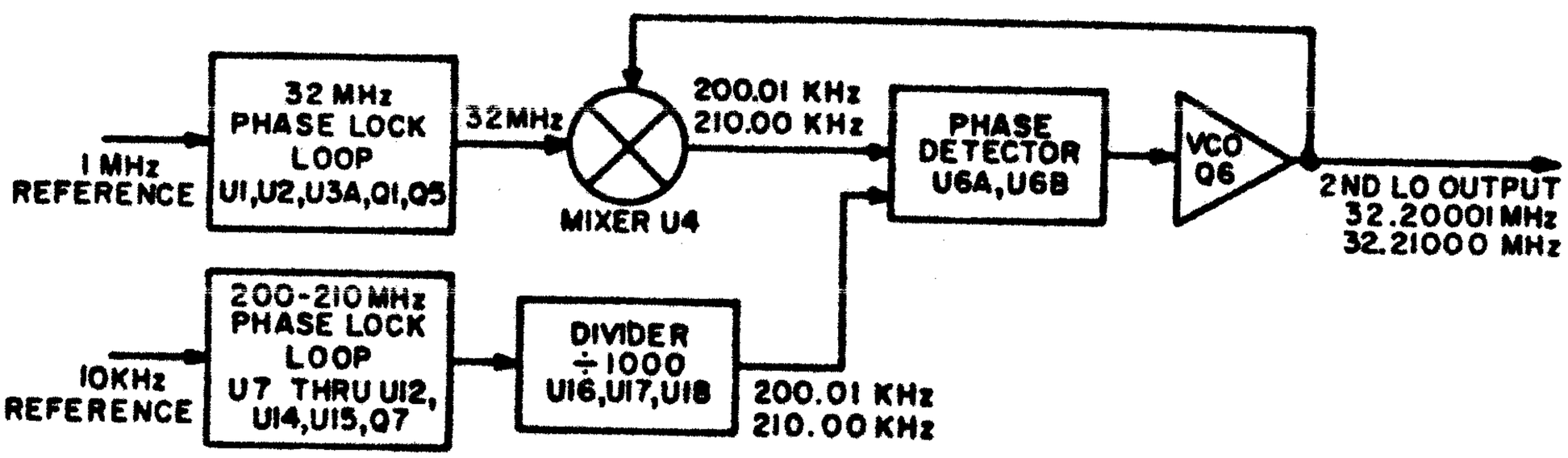


Figure 3-27. 2nd LO Functional Block Diagram

The phase lock loop in the upper left section of the diagram has a reference input of 1 MHz from the Time Base and a fixed output of 32 MHz. The bottom phase lock loop is programmable and produces an output from 200 to 210 MHz. This output routes through a divide-by-1000 stage, resulting in a programmable output from 200 to 210 kHz. The third phase lock loop depends on the other two phase lock loops to produce the 2nd LO output.

An explanation of the 2nd LO output loop will clarify the overall operation of this synthesizer. The 2nd LO output routes to mixer U4, where it is mixed with the fixed-frequency phase lock loop output of 32 MHz. This mixer produces the difference of its two input frequencies, resulting in an output within the 200 to 210 kHz range. This output is amplified and level translated for TTL compatibility. Mixer output and divide-by-1000 output signals are compared in frequency and phase by U6A, whose output characterizes the difference betweenits two inputs. Filter U6B integrates the phase detector output into a varying dc voltage which drives the VCO to establish the desired frequency. The VCO output is sent through a buffer amplifier whose output is the 2nd LO.

3.4.18.2 Circuit Description

The circuit description for the 2nd LO follows the same organization as the functional description. The 2nd LO will be discussed in the following order: 32 MHz phase lock loop, programmable phase lock loop, and 2nd LO output loop. The schematic diagram for the 2nd LO is shown in **Figure 6-18.**

The 32 MHz phase lock loop utilizes the basic phase lock loop configuration shown in **Figure 3-17.** The VCO output (from oscillator Q5) is applied to buffer amplifier Q1. The collector output of Q1 routes through a divide-by-2 counter, U3A, and a divide-by-16 counter, U2, dividing the 32 MHz output down to 1 MHz. This signal and the 1 MHz reference from the time base are compared in phase detector U1A, and filtered in U1B (these circuits are described in **paragraph 3.3.2.4**). The dc voltage from U1B varies the capacitance of varactor diode CR3. Q5s oscillation frequency depends on the tuned circuit incorporating CR3. Q1 is a buffer amplifier which has two outputs isolated from each other. C9 and L9 pass the 32 MHz emitter signal to the mixer while rejecting any harmonics of 32 MHz or any 1 MHz signals from the input of U4. The collector output is returned to the counter to close the loop.

The programmable phase lock loop incorporates a two-modulus prescaler, swallow counter, divider, phase detector, filter, and VCO. The output of this loop, from Q7, feeds into U15 and U16. U14 and U15 form a prescaler whose divide ratios are 100 and 101. **Figure 3-28** illustrates the prescaler operation. Individually, U15 is a divide-by-10 or 11 counter and U14 is a divide-by-10 counter. Cascading the two counters results in divide ratios of 100 and 110. This needs additional modifications. U15 divides by 11 when both E5 and E4 are at a low state. This occurs only during the swallow counting sequence when E4 is held low by U11C. U15 divides by 10 for 90 input pulses from the VCO. Because of this, nine input pulses enter U14 at pin 2. At this point U14s ripple clock output, pin 15, goes low for one input pulse. This enables U15 to divide by 11 once. Therefore, dividing by 10 nine times (9x10) and dividing by 11 once (1x11) results in a divide ratio of 101 (90+11). This division of 101 occurs until the swallow counter (U7 and U8) reaches terminal count. From this point, E4 of U15 remains high until the divider reaches terminal count, thus dividing by 10. U11B and U11C detect the state of the swallow counter while U11D detects the terminal count of the divider.

The swallow counter is comprised of U7 (a decade counter) and U8 (a binary counter). U11A, B, and C form the swallow counter terminal count detector. The counter can be loaded with any number between 00 and 99, inclusive. During a load pulse U7 and U8 are loaded, and the output of the NAND latch formed by U11B and U11C is reset. This low signal is sent to the prescaler control input of U15, causing it to divide by 101. When U8 reaches state 1010, sensed by U11A, the NAND latch will be set causing the prescaler to divide by 100. As soon as U8 is clocked to state 1010, U7 will be in 0000 state because up counting is used. Since detection occurs when U7 is 0 and U8 is 10, the terminal count for the swallow counter is 100.

The main programmable counter consists of binary counters U9 and U10. U11D is used as the detector. U9 can be loaded with any value between 0 and 9, and U10 is always loaded with 2. Since binary counters are used, the 2 loaded in the second digit is not worth 20 (2x10), but is worth 32 (2x16). U11D senses a high level on the QA output of U9 and the minimum/maximum output of U10. The first time this occurs while up counting is when U10 and U9 are in states 15 and 1, respectively. Again the 15 in the second digit is worth 240 (15x16), so the terminal count is 240 + 1 = 241. Each count of the programmable counter is equal to 100 counts of the overall divide chain so the actual terminal count for the programmable counter is 241 x 100 = 24100.

Combining the terminal counts of both counters will yield the overall terminal count. The terminal count for the swallow counter was 100 and for the programmable counter was 24100. Therefore, the terminal count for the whole chain is 100 + 24100 = 24200. The programmable counter is always loaded with 32 plus the input to U9 so the overall chain is loaded with 3200 (32x100) plus the inputs to the three stages.

FIGURE 3-28

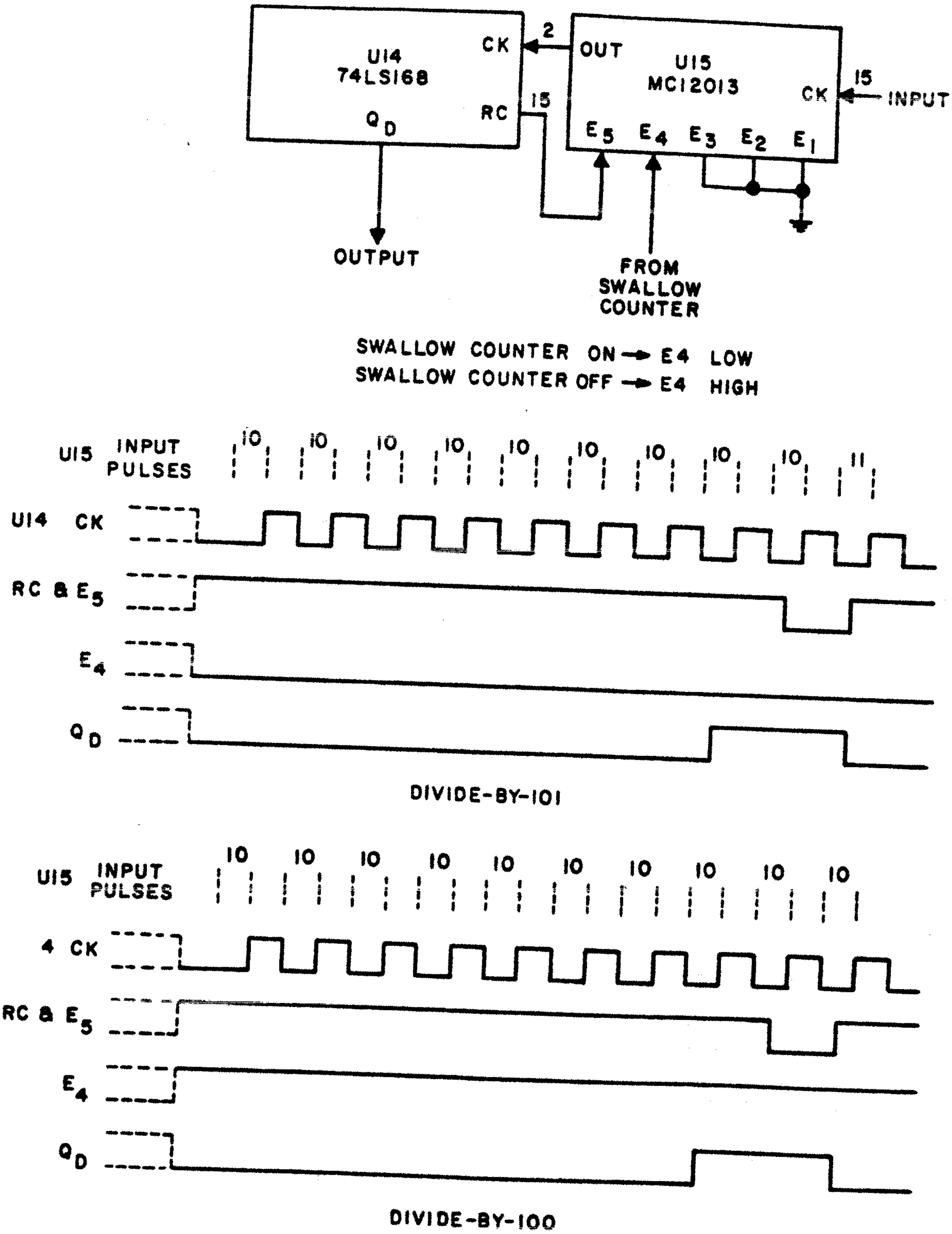


Figure 3-28. 2nd LO Prescaler Timing Diagram

Suppose 000 is loaded into the 2nd LO. The input to the counters is 3200 + 000 = 3200. The terminal count is 24200, so the divide ratio is 24200 - 3200 = 21000. Suppose 999 is loaded. The input is 3200 + 999 = 4199. The divide ratio is 24200 - 4199 = 20001. Suppose 500 is loaded. The input is 3200 + 500 = 3700. The divide ratio is 24200 - 3700 = 20500.

Assuming lock is achieved, a 10 kHz signal should be seen at the output of U11D. This signal is compared to a 10 kHz reference frequency from the Time Base, in phase detector U12A, and filtered in U12B (these circuits are described in **paragraph 3.4.15.4**). The dc voltage from U12B varies the capacitance of varactor CR5 which varies the frequency of oscillator Q7. This signal, ranging from 200.01 MHz to 210.00 MHz, feeds the prescaler and routes to a divide-by-1000 circuit. U16, U17, and U19 each are divide-by-10 counters. When cascaded, the circuit provides a division ratio of 1000 (10x10x10). The input to U6A is a signal ranging from 200.01 kHz to 210.00 kHz.

The 2nd LO output loop produces the 2nd LO frequency range of 32.20001 to 32.2100 MHz in 10 Hz steps. This range of frequencies and the 32 MHz signal from Q1 mix in U4, resulting in a difference frequency range from 200.01 kHz to 210.00 kHz.

Differential amplifier U5 accepts the push-pull output from U4 and amplifies the signal approximately 10 times into a single-ended output. Q2 translates the output level of U5 to TTL levels for the input to U6A. This signal and the phase locked frequency from the programmable divider are compared in phase detector U6A, producing dc voltages that are filtered by U6B (these circuits are described in **paragraph 3.4.15.4**). U6B's output varies the capacitance of varactor diode CR4 and tunes oscillator Q6. This output enters a buffer amplifier, Q3, where the signal is output to mixer U4, and is coupled through impedance matching voltage divider C22, C23, to become the 2nd LO output.

3.4.19 TYPE 791600-1 3RD LO SYNTHESIZER (A5A1A2)

The 3rd LO is part of the 1st and 3rd LO/Time Base board, Type 791600. The 3rd LO has an input of two reference frequencies from the Time Base and a fixed output frequency of 11.155 MHz. The 3rd LO utilizes a basic phase lock loop configuration and a digital mixing technique. A functional description along with a circuit description is provided below.

3.4.19.1 Functional Description

Figure 3-29 shows a functional block diagram of the 3rd LO. Included in the diagram are reference designations that correspond to the 3rd LO schematic. The 3rd LO is part of the 1st and 3rd LO/Time Base schematic diagram, **Figure 6-17**. The VCXO (voltage-controlled crystal oscillator) for this synthesizer is formed by Q8, Y1, CR7, and their associated components. The oscillator is crystal-controlled to 11.155 MHz, and will be driven into proper phase relationship by the dc tuning voltage applied to CR7. The oscillator signal is buffered by emitter-follower Q9 and is split into two signal paths. One path is to board pin A55, the 3rd LO output. The other path is to flip-flop U21B. The flip-flop acts as a digital mixer, producing an output frequency equal to the difference between the VCO frequency (11.155 MHz) and the frequency that is the nearest integral multiple of the clock frequency (223 x 50 kHz = 11.15 MHz). The difference equals 5 kHz. This signal is applied to phase detector U22 along with a 5 kHz reference derived from the Time Base circuit by U21A. The error pulses are integrated into a control voltage for the VCO.

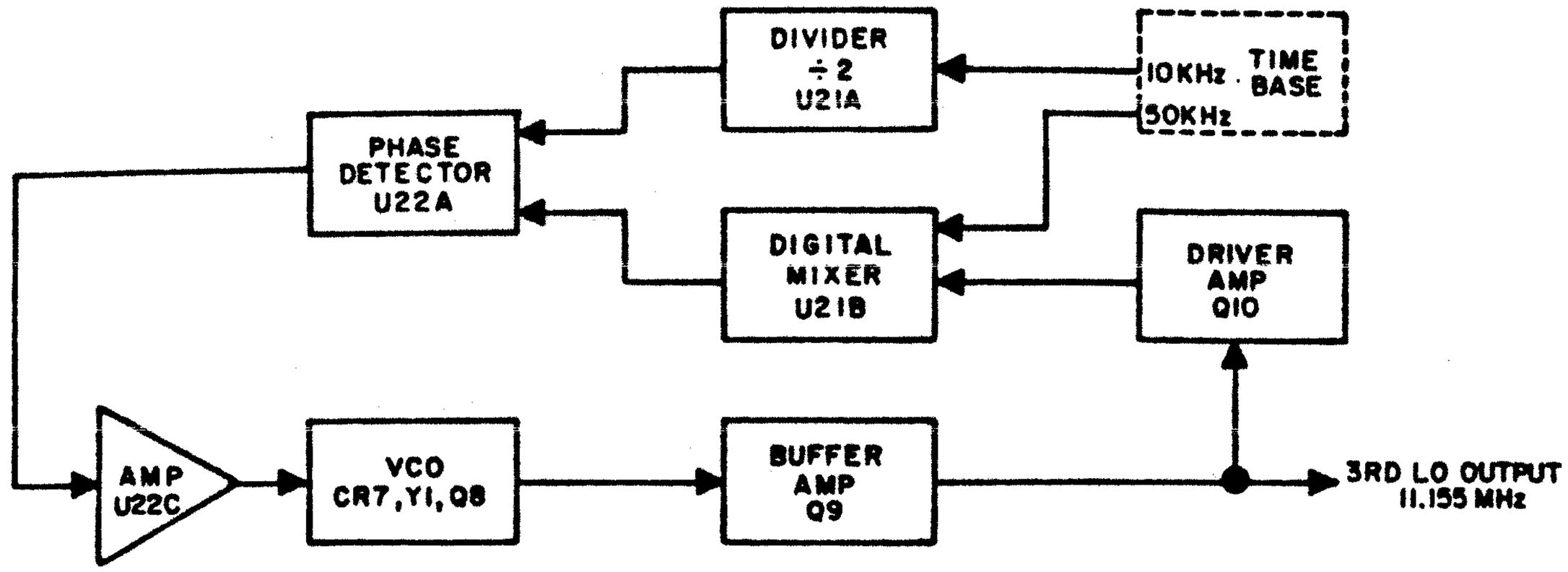


Figure 3-29. 3rd LO Functional Block Diagram.

3.4.19.2 Circuit Description

The 3rd LO output, found at pin A55 of the 1st and 3rd LO Synthesizer board (A5A1A2), is roughly a 100 mV rms sine wave. This signal also couples to Q10, through C37, where it is amplified to levels applicable for the digital mixer. The 3rd LO signal is compared to a 50 kHz reference at pin 11 of U21B, to produce a 5 kHz output, when the 3rd LO is locked. This 5 kHz signal from the mixer is compared to a 5 kHz signal from the time base, via divide-by-2 U21A, in the phase detector, U22A. The charge pump U22B converts the differences in phase and/or frequency into positive and negative going dc levels. These levels pass through filter U22C and bias varactor diode CR7. The 11.155 MHz crystal oscillator is then driven in the direction to achieve lock. The 3rd LO frequency then passes through buffer amplifier Q9 and TTL driver Q10 to complete the loop.

Although the VCO incorporates an 11.155 MHz crystal, Y1, a phase lock loop is still needed. The purpose of the phase lock loop is to vary the oscillator frequency for the purpose of phase-locking it with the Time Base. With the phase lock loop disconnected, the crystal oscillator can produce a usable output frequency for the 3rd LO but would not be exactly the correct frequency to mix with the 10.7 MHz output of the 2nd Mixer.

3.4.20 TYPE 791576-1 BFO SYNTHESIZER (A5A3)

3.4.20.1 Functional Description

The BFO Synthesizer produces a 455 kHz ±8.9 kHz signal. The BFO therefore tunes from 446.1 to 463.9 kHz, in 100 Hz steps. This synthesizer utilizes the basic phase lock loop configuration shown in **Figure 3-17.** The actual phase lock loop operates at a frequency range of 10 times the BFO output to allow for the use of a 1 kHz reference frequency.

A functional block diagram of the BFO Synthesizer is shown in **Figure 3-30.** Some reference designations are included in the diagram and correlate with the BFO schematic diagram, **Figure 6-19.** The functional block diagram does not include all external connections and should only be used with this discussion.

The VCO produces a frequency that is distributed to the BFO output connection (via divide-by-10 counter U10) and to the programmable counter clock inputs. The presettable inputs, in conjunction with the end of cycle detector, create a divide-by-N counter. The end of cycle detector produces pulses which are compared to a 1 kHz reference frequency in the phase detector. The resultant output is pulses that characterize the difference in frequency and phase of the two input frequencies. The loop filter takes the output pulses from the phase detector and integrates them into a varying dc voltage. This varying voltage drives the VCO in the proper direction to establish the desired frequency.

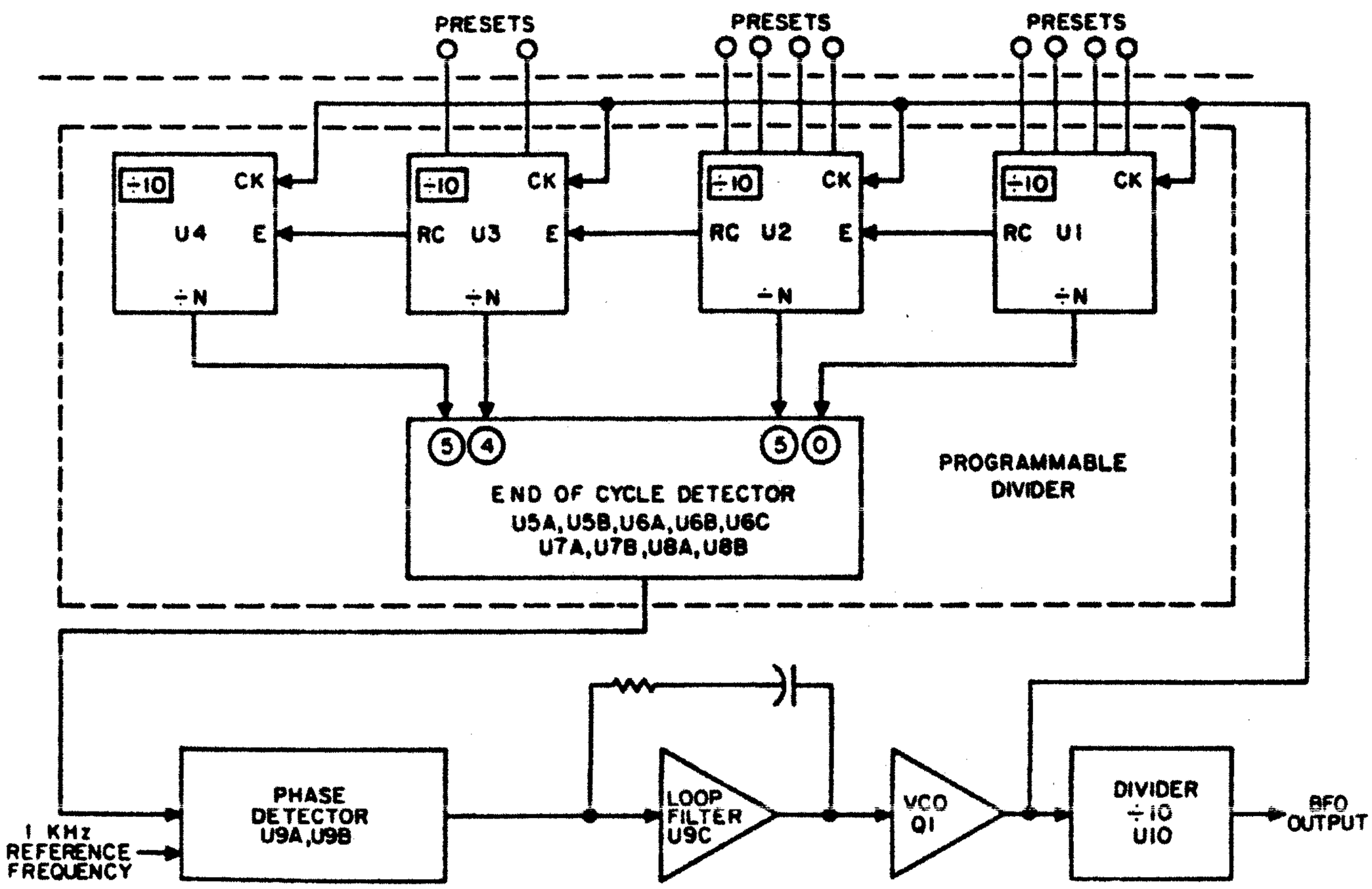


Figure 3-30. BFO Functional Block Diagram

3.4.20.2 **Circuit Description**

The circuit description of the BFO Synthesizer is presented in a sequential manner to facilitate understanding. The BFO phase lock loop will be discussed in the following order: programmable divider, phase detector, charge pump, loop filter, and VCO. Integrated circuit data is supplied where needed. The BFO Synthesizer schematic diagram is shown in **Figure 6-19.**

Refer to **Figure 3-30** to aid in the description of the counters used in the programmable divider. U1, U2, U3, and U4 are BCD synchronous up/down counters. These counters may be programmed, through inputs D, C, B and A, for any initial state, 0 through 9. The ripple clock output and count enable input permit cascading. The ripple clock output, normally high, produces a low level pulse when the counter is at 9 when counting up, and at 0 when counting down. A high at the enable input inhibits counting while a low level input enables counting. The direction of count is determined by the level of the up/down (U/D) input. When low, the counter counts up, and when high, it counts down. The preset function is controlled by the state of the load inputs. When a logic low is applied to the load input, the BCD number at the preset inputs (D, C, B and A) is loaded into the counter, and counting will begin from that number.

The programmable divider must produce an output of 1 kHz for any input signal in the range of 4.461 to 4.639 MHz. Therefore, the divide ratio of the programmable counter must be from 4461 (4.461 MHz+1 kHz) to 4639 (4.639 MHz+1 kHz). Because counters U1 through U4 are cascaded (by connecting the ripple clock of one to the enable of another) and have a maximum count of 10000 (10x10x10x10), additional circuitry is needed to reduce the divide ratio.

To reduce the maximum count, an end-of-cycle detector circuit is used to terminate the count sequence. The end-of-cycle detector, consisting of U5A, U5B, U6A, U6B, U6C, U7A, and U7B terminates the counting of U4, U3, U2, and U1 at 5450. When this number is detected, a pulse is sent to the phase detector (U9) and the counters are reset.

Now that a terminal count has been established, an explanation of the presettable inputs follows. The preset of U4 is always set (hard wired) to 0000. U3 has two preset inputs which depend on the direction of counting. These inputs to U3 connect to the plus or minus (±) thumbwheel switch for variable BFO selection. Selecting a negative (-) BFO frequency enters a 1001 into U3 and the counters count up. Selecting a positive (+) BFO frequency enters a 0000 into U3 and the counters count down. U2 has nine possible preset input states from BCD 0000 to 1000. U1 has ten possible preset states from 0000 to 1001. These possible preset states are determined by the setting of the BFO switch. Selecting a zero BFO offset (±0.0 kHz) grounds all preset inputs of U1 and U2, loading both counters with 0000. Also, selecting a "0" from the "+, 0, -" thumbwheel grounds all thumbwheel preset inputs causing a zero BFO offset. In all sideband modes, the BFO offset line is grounded, in turn grounding the presets of U1 and U2 and loading them with 0000. Refer to the BFO Switch Truth Table, **Table 3-9**, for further clarification of the BFO Switch operation.

Knowing the possible input values of the divider and the end-of-cycle detection number, an example will help explain the count sequence (refer to **Figure 6-18**). Assume that counters U4, U3, U2, and U1 are all loaded with 0000. This corresponds to a BFO frequency of 455 kHz, a VCO frequency of 4.55 MHz, and a BFO thumbwheel setting of 0.0 kHz. A "+" thumbwheel setting initiates down counting. Therefore, counting from 0000 down to 5450 results in a divide ratio of 4550. (Note that the next count down from 0000 is 9999). With a divide ratio of 4550, the counters will reach a terminal count 1000 times a second with an input frequency of 4.55 MHz.

Notice that setting the thumbwheel switches to -0.0 kHz indicates the same VCO frequency, 4.55 MHz, but initiates "up" counting. A negative "-" setting enters a 1001 (BCD 9) in U3, making the count start from 0900. With an input of 0900 counting up to 5450 results in the same divide ratio of 4550.

Assume a BFO frequency of 460.4 kHz is needed. This corresponds to a thumbwheel selection of +5.4 kHz, and a VCO frequency of 4.604 MHz. From the thumbwheel selection, a "+" presets U3 with a 0000, a "5" presets U2 with a 0101, and a "4" presets U1 with a 0100. Therefore, counting from 0054 down to 5450 results in a divide ratio of 4604. With a divide ratio of 4604, the counters will reach terminal count 1000 times a second with an input frequency of 4.604 MHz.

U8A and U8B have two purposes: to send a pulse to the LOAD input of the counters for presetting and to extend the width of the end of cycle detector's pulse.

The phase detector, U9A, receives a fixed 1 kHz frequency at its reference input, pin 1, and a signal from the divider at its variable input, pin 3. These two signals produce an output that characterizes their differences in frequency and phase. The charge pump, U9B receives this pulsed waveform from the phase detector outputs and translates them to fixed positive and negative-going amplitude levels (centered about 1.5 V).

These levels are filtered and integrated by the loop filter, Q4 and U9C, providing the tuning voltage for the VCO. A more complete description of the phase detector can be found in **paragraph 3.4.15.4.**

Buffer Q4 provides a high-input impedance for the preceeding stage. Positive and negative going pulses at the gate are developed across the source output and applied to inverting amplifier U9C. The output of U9C is coupled back to the gate of Q4, through R3 and C1, providing the integrating action. Potentiometer R1 establishes zero gate to source voltage (Vgs) to Q4.

Emitter-coupled oscillator Q1 with its external tank circuit comprises the VCO. Varactor diode CR1 receives a control voltage from the active filter and adjusts the tank circuit's frequency of oscillation to establish lock. The VCO operates from 4.461 to 4.639 MHz. Resistors R8, R9, and R10 form the dc bias network, and feedback capacitor C7 sustains oscillation along with tuned circuit C8 and L1. R11 and C9 form a low-pass filter for +15 V isolation, and the VCO's output is coupled to the next stage by C10.

Q2 and its surrounding components form a tuned amplifier for the incoming VCO output frequency. This VCO sine-wave frequency is then coupled to a sine-wave to TTL converter, Q3. From here, the digital signal returns as the clock input of the programmable divider, and is divided by 10 in U10 and provided as the BFO output signal.

3.4.21 TYPE 791600-1 TIME BASE CIRCUITS (A5A1A2)

The Time Base circuits are part of the Type 791600 board, A5A1A2. The Time Base circuits have two sources of reference from which to choose. A functional description is given along with the functional block diagram shown in **Figure 3-31.** Reference designations are included in the diagram and correlate with the Time Base portion of the 1st and 3rd LO/Time Base Schematic, **Figure 6-17.**

3.4.21.1 Functional Description

The Time Base can be controlled internally with a 2 MHz temperature compensated crystal oscillator (TCXO) and divide-by-2 frequency divider, or witha 1 MHz external source.

This 1 MHz reference is divided down to 50 kHz, 40 kHz, 10 kHz, and 1 kHz. Buffer amplifiers Q6 and Q7 are used for isolation purposes. Synthesizers that need certain reference frequencies are listed below each frequency in the diagram. Refer to the schematic diagram in **Figure 6-17.** S2 in **Figure 3-31** represents the function of U23.

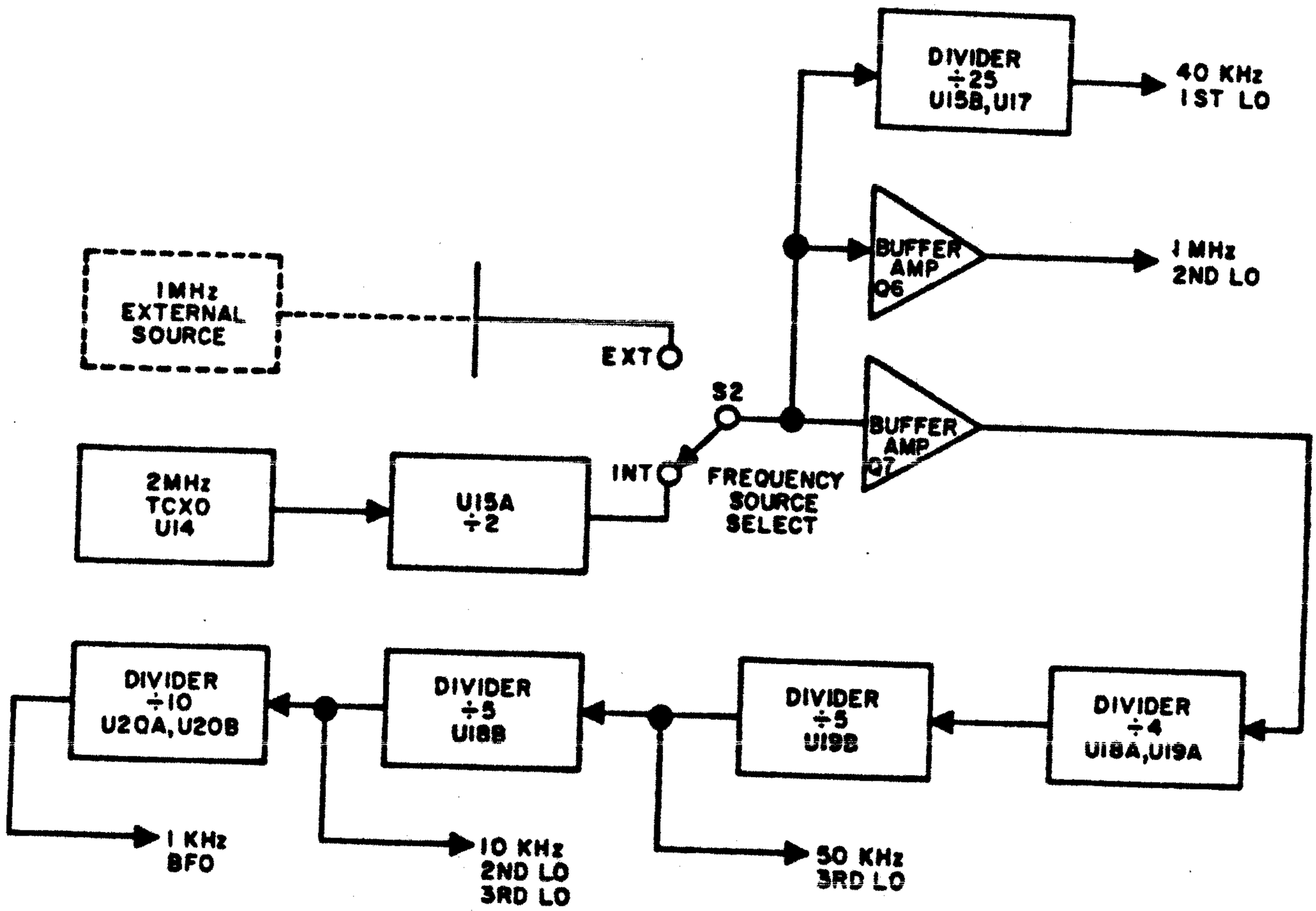
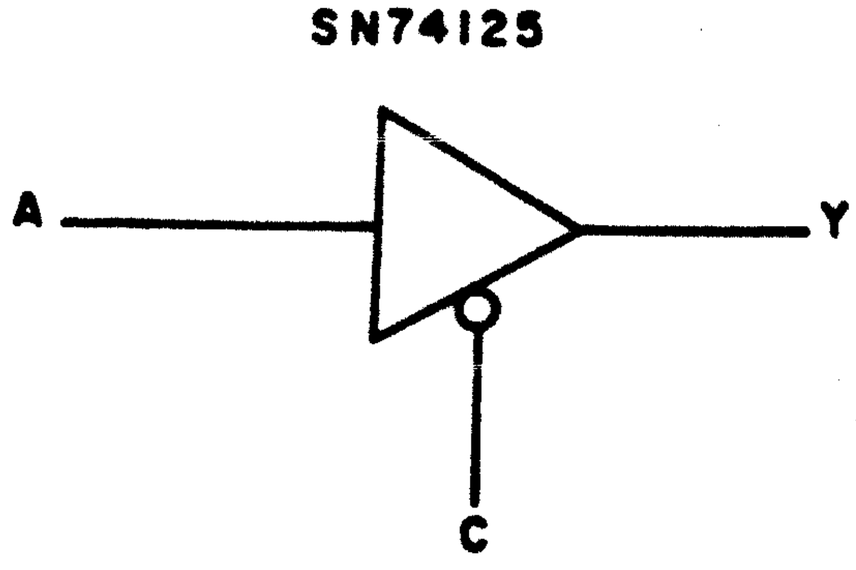


Figure 3-31. Time Base Circuits Functional Block Diagram

3.4.21.2 **Circuit Description**

An internal source of reference is provided by a 2 MHz TCXO, while an external source of reference must be a 1 MHz signal of approximately 50 mV. Tri-state buffers accomplish the switching of internal and external reference sources. A truth table of the tri-state buffers used is given in **Figure 3-32.** Getting information from input A to output Y depends upon the state of input C. Information passes from input A to output Y when the state of input C is low. Similarly, information is inhibited from the output when the state of input C is high.

When operating with an external source of reference, the external select (EXT SEL) line is grounded and the internal select (INT SEL) is pulled high by R84, and the externally supplied 1 MHz reference is seen at module pin A17, EXT/INT STD. The internal 1 MHz reference is inhibited when it reaches tri-state buffer U23B. Therefore, the only source for the 1 MHz signal to transformer T1 is the external one. T1 and C23 resonate at 1 MHz while the voltage divider of R34 and R35 shifts the 1 MHz signal to a 2.5 Vdc level. This signal enters U16 which converts the sine wave to TTL levels. The output of U16 passes through tri-state buffer U23A and on to the rest of the Time Base circuits.



U23A
U23B
U23C

TRUTH TABLE

INPUTS		OUTPUTS
A	C	Y
H	L	H
L	L	L
X	H	HI-Z

Figure 3-32. Tri-State Buffers

Operation with the internal source grounds the internal select (INT SEL) line and allows the external select line to be pulled up by R85. Tri-state buffer U23 allows the 2 MHz signal that is divided to 1 MHz to be passed on to the rest of the circuitry. The 1 MHz reference splits to two parts of the circuit. In one direction, the reference signal passes through U23C and out the EXT/INT STD connection. The signal does continue to pass through U16 but is inhibited at U23A. In the other direction, the reference signal passes to pin 3 of U23A (EXT) or pin 11 of U23B (INT), and on to the rest of the time base circuitry.

For either source of reference, a 1 MHz TTL signal is present at the input of Q6 and U15B. This signal is divided by 25, through U15B and U17, to become a 40 kHz reference for the 1st LO. The 1 MHz signal also passes through an isolation amplifier Q6 to board pin A9 to be used as a reference for the 2nd LO. The 1 MHz signal also passes through another isolation amplifier, Q7, to be divided down to three more reference frequencies.

U18A and U19A form a divide-by-4 network whose input is 1 MHz and whose output is 250 kHz. This 250 kHz divides down to 50 kHz through divider U19B and is sent to U21B, the digital mixer of the 3rd LO. The output of U19B also enters U18B, whose output is a 10 kHz signal. This signal leaves the board to be used as a reference for the 2nd LO, and is divided to 5 kHz by U21A to act as a reference for the 3rd LO circuit. The 10 kHz signal also passes through a divide-by-10 network, consisting of U20A and U20B, for an output reference signal of 1 kHz.

3.4.22 TYPE 791630-1 1ST AND 3RD LO SYNTHESIZER/TIME BASE (A5A1)

This assembly is located in the right-hand side of the receiver and connects the 1st and 3rd LO/Time Base circuit board to the 1st LO VCO circuit board. The connections include three lines for the VCO band select code, two lines for the VCO tuning voltage, and one line connecting the VCO output to the 1st LO divider section. Also on this board is a -12 Vdc regulator that supplies voltage to both the 1st LO Synthesizer and the 1st LO VCO.

The schematic diagram corresponding to this circuit board is shown in **Figure 6-15.** The tuning voltage connects to the VCO through a 40 kHz trap (C1, C3, L1, L2, and L3) and a low-pass filter (C4, C6, C8, R4, and 14). CR1, CR2, and CR3 provide a 1.8 V potential on the tuning voltage reference line. A -15 Vdc potential from the 1st LO circuit board enters pin 3 of the voltage regulator VR1 and is regulated to a -12 Vdc output on pin 2. The -12 Vdc is supplied to the VCO, to power its circuits, and to the 1st LO Synthesizer to power lead-lag filter U7 and the band switching circuit.

3.4.23 TYPE 791575-1 MANUAL TUNING UP/DOWN COUNTER (A6A1)

The Manual Tuning Up/Down Counter contains the RF frequency data. This information is sent to the 1st and 2nd LO Synthesizers, and is encoded for multiplexing to the display board. The frequency data can be changed in two ways: from the Manual Tuning Module via front panel control, or from the Remote Input Jack by an external controller. A block diagram of the Up/Down Counter is shown in **Figure 3-33.** The functions of the Up/Down Counters and the multiplexer are presented below followed by an overall circuit description.

3.4.23.1 Integrated Circuit Data

The 14510 is a presetable up/down decade counter and is shown in **Figure 3-34.** Pin 15 is the clock input. The counter will increment for each rising edge of the clock when the up/down input (pin 10) is high; when pin 10 is low, the counter will decrement. If the parallel enable input (pin 1) is high, clocking is inhibited and the information on the P inputs are transferred to the corresponding Q outputs. Cascading of counters is accomplished by tying the carry input (pin 5) of one counter to the carry output (pin 2) of the preceding counter and by connecting the control inputs (clock, up/down, parallel enable) in parallel. If the carry input is high, the counter is inhibited from clocking. The carry output, normally high, goes low during a carry condition. Carry conditions occur when the counter is in a 0 state during down counting or when the counter is in a 9 state during up counting. Therefore, any stage in a counter chain will clock only when all preceding stages are in a carry condition.

The 14512 is an eight-input data selector and is shown in **Figure 3-34.** Control inputs A, B, and C select which of the data inputs, X_0 to X_7, is gated to output Z. The data input selected is determined by the binary equivalent of the control inputs. When activated, the disable line will force a low on the Z output and the inhibit input will cause it to go to the high impedance state. Inhibit and disable inputs are not used in this application.

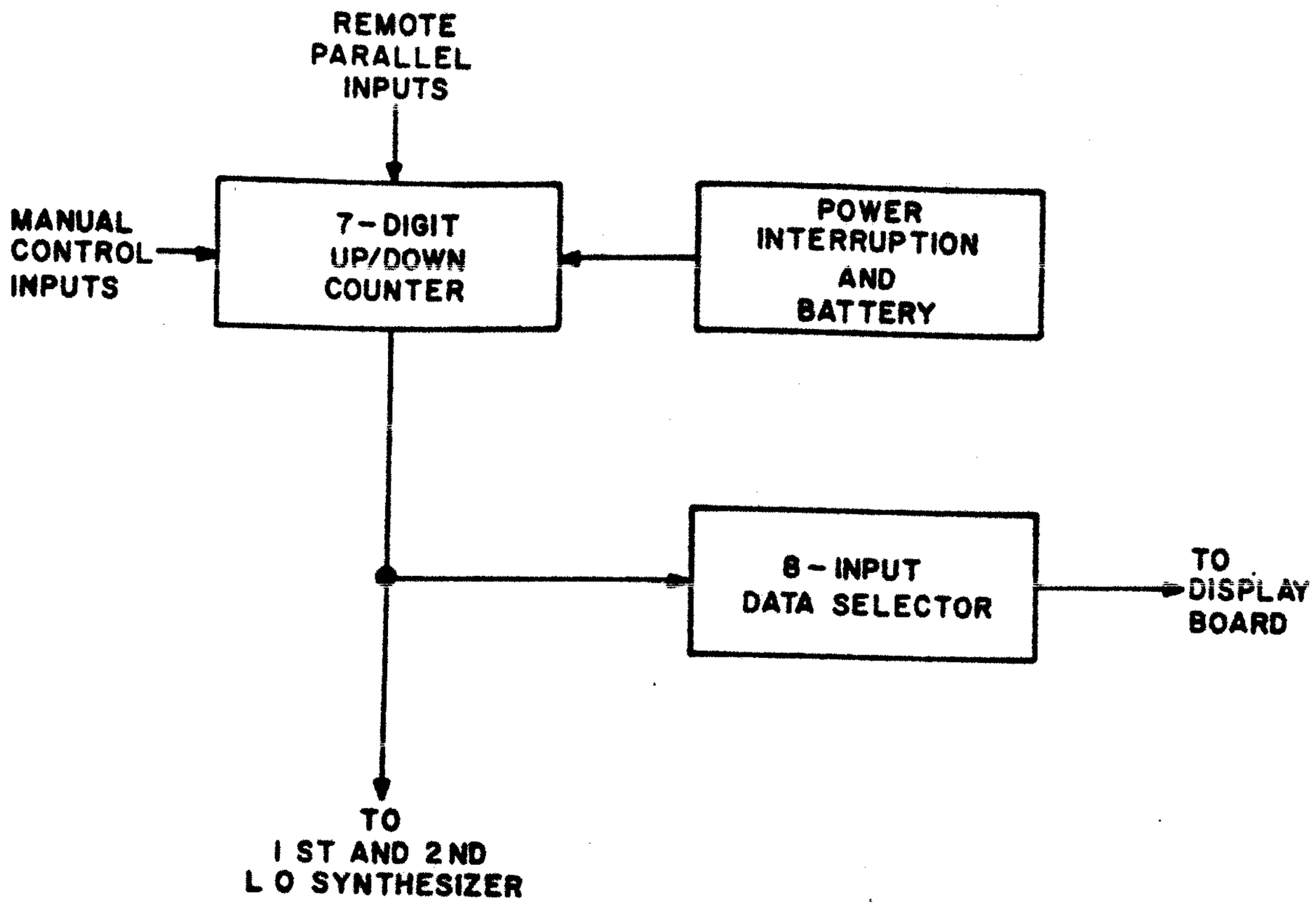


Figure 3-33. Manual Tuning Up/Down Counter Block Diagram

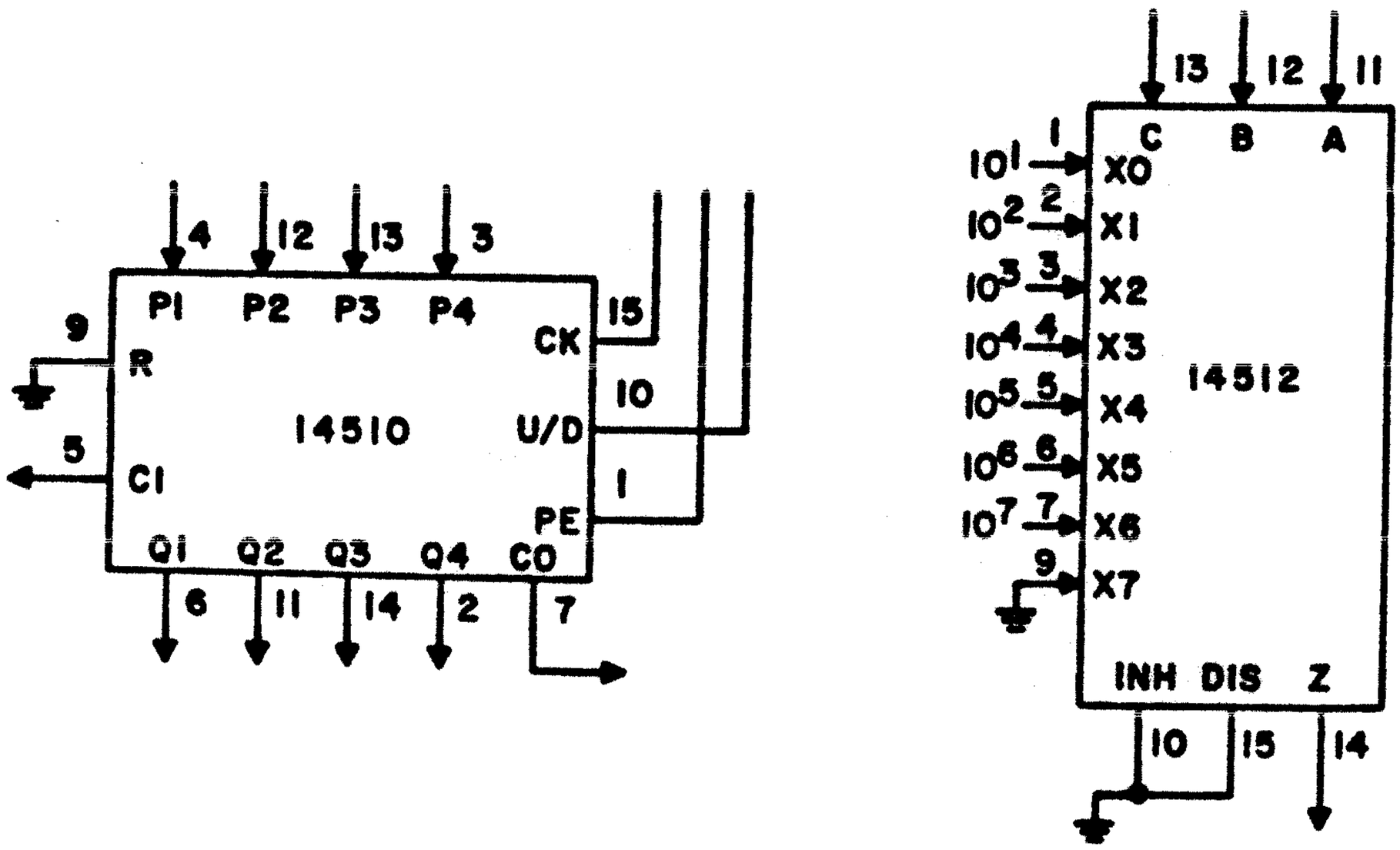


Figure 3-34. Up/Down Counter Integrated Circuit Data

3.4.23.2 Circuit Description

The schematic diagram for this circuit is shown in **Figure 6-21**. The Up/Down Counter is comprised of U2 through U11. U2 through U7 are MC14510s cascaded to form a six-digit presettable up/down decade counter. U1F, U8C, U9, U10, and U11 form the last stage of the counter. U9 is a dual JK flip-flop. U1F, U8C, U18B, U10B, and U10D form the logic to control the states of U9. During up counting, U9 will clock from 0 to 2 and then back to 0 again. Down counting will produce states in the opposite direction. U11, U10C, and U10A form the logic to preset U9. With the remote frequency load line low, the outputs of U11 will all be low, having no effect on U9. If the load line is high, U9A will reset if the 2^0 of 10^7 input is high and clear if it is low; U9B will reset if 2^1 of 10^7 is high and clear if it is low. U8A, U8B, and U8D are used to gate the carry outputs of the first three stages to be used for the tuning resolution select. The tuning resolution switches provide a short to the step select switch output (normally low) for the activated switch and an open circuit for the switches not chosen. Resistors R5 to R8 are pull-up resistors to provide a high level on the open circuited lines. If the 10^1 switch is selected, counter U2 will be enabled. Since the other lines will all be high, all AND gates will be enabled. The resultant is a normal seven decade counter. If the 10^2 step select is chosen, AND gate U8D will be disabled. U2 will be inhibited since its carry input will be high. Since the carry input of U3 is now always low, it will clock for each pulse received on its clock input. U8B and U8A will still be enabled allowing for normal carry operation. The counter now behaves as though counter U2 is no longer in the circuit. If the 10^3 select is chosen, both U2 and U3 are disabled; if the 10^4 is chosen, U2, U3, and U4 are disabled.

The clock and direction signals are from the Manual Tuning Module. When up counting is desired, the clock line lags the direction line by 90°; when down counting is desired, it leads by 90°. U1A and U1E are Schmitt triggers to buffer the input signals. Since both clock and direction lines are inverted, the relative sense between the two signals is maintained. During up counting, the rising edge of the clock will always occur when the direction line is high, causing the counter to increment. In down counting, the rising edge will always occur when the direction line is low, decrementing the counter.

The P inputs of the counters are connected to the Remote Input Jack, J1. When the remote frequency load line is pulsed high, the levels on the P lines will be transferred to the outputs of the counter. If the load line returns low the counter will resume clocking from the new data. The Remote Input Jack also contains lines from the IF bandwidth select circuitry. This allows remote control/monitor of the IF BW.

The RF frequency information is sent to the 1st and 2nd LO Synthesizers via the I/O and Synthesizer Motherboards. It is also sent to multiplexers U12 to U15. U12 receives the 2^0 bit of each digit, U13 receives the 2^1 bit, U19 received the 2^2 bit, and U15 receives the 2^3 bit. The control inputs out U12 to U15 are all tied in parallel and feed to a binary counter U16. This counter is continuously clocked from an oscillator formed by U1C, U1B, C2, and R14. The frequency of oscillation is approximately 2.3 kHz. The outputs of U16 are also sent to J2 for decoding on the display board. The outputs of U12 to U15 are buffered by U17.

Operation of the data selector is as follows: when the counter U16 has all zeros on its outputs, the A, B, and C inputs of U12 to U15 will be low. This will gate all X_0 inputs to their respective Z outputs. The information sent to the display board via J2 will be:

If $Q_2\ Q_1\ Q_0 = 000$, then:

$2^3\ 2^2\ 2^1\ 2^0 = 10^1$ Digit

When the oscillator clocks U16 again, the outputs will become 001. This will cause the X_1 input of each multiplexer to appear at its respective Z output. As the counter U16 clocks, all X inputs will be sent to the Z output in the code shown in **Table 3-8.**

Table 3-8. Data Selector 14512, Digit Control Codes

Q_2	Q_1	Q_0	$2^3\ 2^2\ 2^1\ 2^0$
0	0	0	10^1 Digit
0	0	1	10^2 Digit
0	1	0	10^3 Digit
0	1	1	10^4 Digit
1	0	0	10^5 Digit
1	0	1	10^6 Digit
1	1	0	10^7 Digit
1	1	1	All Low

This information can now be decoded on the display board. The display board determines which digit is present on the 2^3, 2^2, 2^1, and 2^0 lines by decoding the Q_2, Q_1, and Q_0 inputs.

During power down, the RF frequency is remembered by powering the Up/Down Counter from BT1 (2.5 V) mounted on the receiver rear panel. Diode CR1 is used to charge the Nicad battery when power is on and to isolate the battery from the rest of the receiver when power is down. It is a hot carrier diode, dropping only about 0.4 V when forward biased. When power is on, V_{DD} is at 5 V, forward biasing the diode and charging the battery through R9. If power fails, V_{DD} drops to 0 V and diode CR1 becomes reverse biased, allowing battery current to flow only to the chips connected to V_{DD2}.

The purpose of Q1 and its circuitry is to inhibit all counters when power down occurs. Without it, the counters could clock when power was again applied to the encoder assembly, because the clock input could go from a low (during power down) to a high (during power up).

Transistor Q1 controls the step select switch ground. When power is on, the 10 V across voltage divider R11 and R12 will turn Q1 on, which will place a low on the step select common. If the 10 V line drops below 7 V, the base of Q1 will drop below 0.7 V, and the transistor will turn off placing a high on the step select common through resistor R10. This high will prevent any of the step select lines from going low. The step select button chosen will short to a high level now, not a low, and the unchosen switches will still be pulled high by resistors R5 through R8.

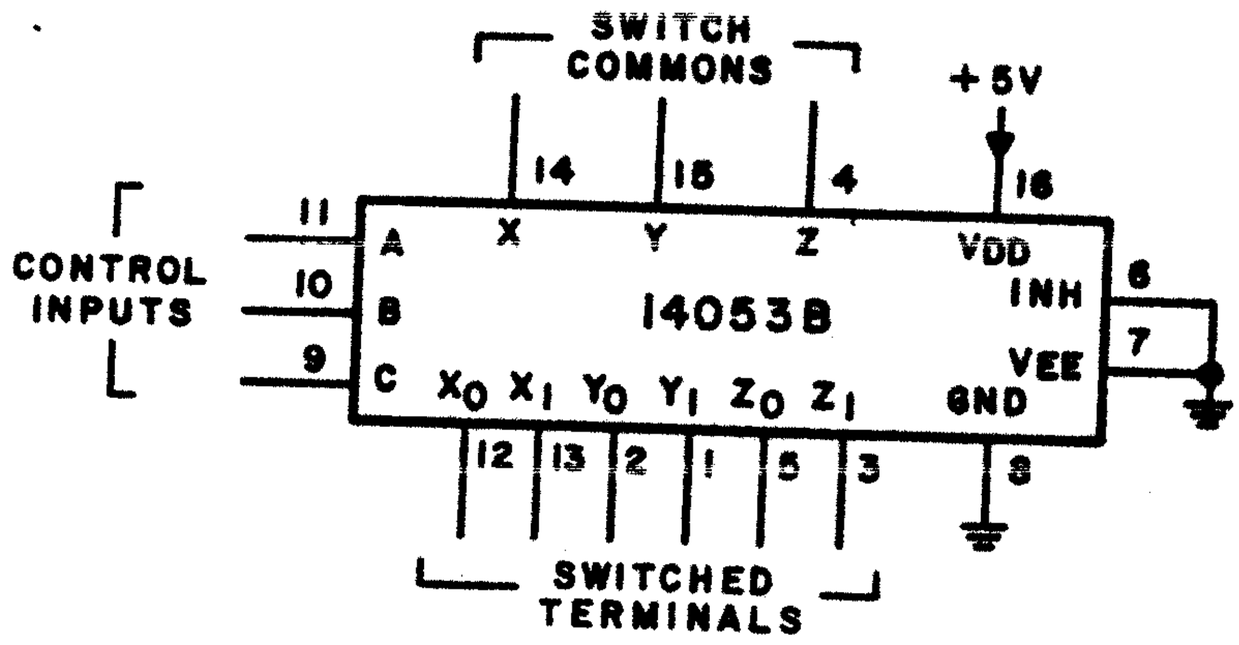
3.4.24 TYPE 791828-1 FRONT PANEL INTERCONNECT (A6A2)

This module translates information received from the manually controlled front panel into control information for the receiver. Front panel information entering this module controls detection mode, gain mode, meter mode, and IF bandwidth, in addition to headphone and RF gain levels. This information is then decoded, for use primarily in the IF stages of the receiver. Two output lines from the Front Panel Interconnect, however, control the BFO. The schematic diagram for this module is contained in the Front Panel Interconnect Schematic Diagram, **Figure 6-22.** I/O Motherboard Schematic Diagram, **Figure 6-20**, and Receiver Main Chassis Schematic Diagram, **Figure 6-25**, should be referred to as an aid in understanding Front Panel Interconnect Operation.

This circuit description will explain the operation of each manually-controlled input to this module and how it decodes and sends the information to the IF and BFO circuits. The Front Panel Interconnect board incorporates two integrated circuits, U1 and U2, which will be discussed below.

As can be seen from the schematic diagrams, most of the lines from the front panel are simply passed through to the rest of the receiver. For these lines, this module serves as a patch panel. For the IF bandwidth lines and certain detection mode lines, diode logic is performed by CR1-3, CR5-10 and U2 to control the combinations of IF filters, as described in **paragraph 3.3.3.9.**

The truth table for analog multiplexers U1 and U2 is shown in **Figure 3-35.** This IC performs as three digitally controlled SPDT switches. When control input A is logic low, terminals X and X_0 are internally connected. When A is logic high, X and X_1 are connected. Similarly, input B controls Y, Y_0, and Y_1 and input C controls Z, Z_0, and Z_1. This circuit performs most of the logic functions associated with the front panel pushbuttons for detection mode (on A10A1) and IF bandwidth (on A10A2). Refer to **Figures 6-20, 6-22** and **6-25** for the following descriptions. Notice that both A10A1 and A10A2 have their own set of "E" terminals to A10P1, using some of the same numbers.



CONTROL INPUTS			ON SWITCHES		
C	B	A			
0	0	0	Z_0	Y_0	X_0
0	0	1	Z_0	Y_0	X_1
0	1	0	Z_0	Y_1	X_0
0	1	1	Z_0	Y_1	X_1
1	0	0	Z_1	Y_0	X_0
1	0	1	Z_1	Y_0	X_1
1	1	1	Z_1	Y_1	X_0
1	1	1	Z_1	Y_1	X_1

Figure 3-35. Front Panel Interconnect Integrated Circuit Data

When CW mode is selected, the detection mode switch connects E4 to E12, and E5 to E6. This places +5 V on the CW select line to IF Motherboard A4. Input B of U1 is controlled

by the remote bandwidth control line entering at XA2 pin 11. Since this line is logic low in local mode, U1 input B is normally low, and Y is connected to Y_0. Therefore, when E5 is connected to E6, the +5 V at U1 input A causes the +5 V line at X to be connected through X1, Y_0, and Y, to E19 and the IF bandwidth switch common line, enabling these switches. Therefore, any bandwidth may be selected in CW mode. If "0" is selected on the "+, 0 ,-" BFO switch, the switch common (ground) places a low on U1 input C, Z and Z_0 are connected, Q1 is turned off, and the resulting low voltage at XA2 pin 58 causes the BFO preset lines to be pulled low, producing a fixed 455 kHz BFO frequency. (Refer to **paragraph 3.4.20** for a description of the BFO presets.) If "+" or "-" is selected, the ground is removed and U1 input C is pulled high by R7, Q1 is turned on and power is applied to the BFO preset pull-up resistors, entering whatever frequency code is present at the BFO Switch. Therefore, the BFO may be either fixed or variable in the CW mode.

When AM mode is selected, the detection mode switch connects E4 to E16, and E5 and E14 to E6. This places +5 V on the AM select line (to A4) and allows +5 V on the bandwidth switch common line, enabling these switches. This also places +5 V on XA2 pin 60, which inhibits BFO operation.

When FM mode is selected, the detection mode switch connects E4 to E15, and E5 and E14 to E6. This places +5 V on the FM select line (to A4), enables the bandwidth switches and inhibits the BFO, as previously described.

When USB mode is selected, the detection mode switch connects E4 to E8 and grounds E5 and E14. This places +5 V on the USB select line (to A4) and places a low at U1 input A. This disables the IF bandwidth switches and turns off Q1, fixing the BFO at 455 kHz, as previously described.

When LSB mode is selected, the detection mode switch connects E4 to E7 and grounds E5 and E14. This places +5 V on the LSB select line, disables the IF bandwidth switches and fixes the BFO at 455 kHz.

When ISB mode is selected, the detection mode switch connects E4 to E11, E9 to E10, and opens the normal connection between E10 and E13. Connecting E4 to E11 places +5 V on the ISB select line to A4. In all other modes, the combined audio line is supplied to both audio amplifiers on A10A2, via E9 and E3. In ISB mode, the combined audio line to A10A2E9 is replaced by the ISB/LSB audio line, via the E9-E10 connection. Therefore, the USB audio is supplied to A10A2 headphone amplifier U1A via the combined audio line, and the LSB audio is supplied to amplifier U1B.

Integrated circuit U2 acts to control the routing of Bandwidth Select Voltages (see **paragraph 3.3.3.9**) during normal operation of the bandwidth select buttons. If any BW other than 0.3 or 1.0 kHz is selected, the A and B inputs to U2 are low. This connects X to X_0 and Y to Y_0, effectively connecting the cathodes of CR7 and CR8. Selection of 3.2 or 6 kHz BW will automatically select the wide position of A4A3 through CR7 and CR8 and XA2-49. Selection of 1.0 or 0.3 kHz BW brings the A or B input of U2 high, effectively disconnecting CR7 from CR8. At the same time, the 3.2 kHz position of A4A1 is selected by CR5 or CR6 through XA2-55.

3.4.25 TYPE 791874-1 MANUAL TUNING MODULE (A7)

The Manual Tuning Module controls the direction and rate of change of the tuned frequency. This module connects to the Manual Tuning Up/Down Counter (A6A1) and is

mounted behind the receiver front panel. The Manual Tuning Module consists of two parts: the encoder assembly and the Tuning Resolution switches. The schematic diagram of this module can be found in **Figure 6-21.**

3.4.25.1 Type 791589 Tuning Resolution (A7A1)

The Tuning Resolution switches select the desired tuning step to be used. The tuning steps are: 10 Hz, 100 Hz, 1 kHz, and 10 kHz. Switching is accomplished by connecting the desired tuning step to the step select switch line (+5 V) of the Manual Tuning Up/Down Counter board (A6A1). The schematic diagram for this circuit is shown in **Figure 6-25.**

When the 10 Hz button is depressed, E2 (10 Hz step line) connects to E16 (+5 V) and all digits are available for tuning. When the 100 Hz button is depressed, E10 (the 100 Hz step line) connects to E16 (+5 V). The 10 Hz digit is locked to the frequency indicated when the 100 Hz button was engaged, while all other digits are available for tuning. When the 1 kHz button is depressed, E12 connects to E16, thus the five most significant digits of the readout can be varied by the tuning knob. The two least significant digits will be locked to the frequency indicated when this button is engaged. When the 10 kHz button is selected, E8 connects to E16 and only the four most-significant digits of the readout can be varied by the tuning knob. The 1 kHz, 100 Hz, and 10 Hz digits will be locked to the frequency indicated when the 10 kHz button is engaged.

When the tuning disable button is engaged, the receiver locks to the frequency currently being displayed, any other tuning button will be released, manual tuning is disabled, and remote frequency control is enabled through A6A1.

3.4.25.2 Encoder Assembly (A7U1)

This assembly converts tuning knob rotation to digital pulses for the Manual Tuning Up/Down Counter. When the tuning knob is turned, each of the two output lines from the encoder will swing repeatedly between approximately +5 V and 0 V. If the knob is rotated at constant speed, these two outputs will appear as trains of square waves. Due to the internal mechanics of the encoder, the transitions of these two wave trains will be staggered in time with respect to each other. When the knob is rotated clockwise to increase tuned frequency, the square wave on the direction line will appear to lead that on the clock line as in **Figure 3-36.** The action of the up/down counter depends on the level of its up/down input at the instant its clock line goes high. The level of the up/down input at any other time has no effect. Therefore, clockwise rotation causes the counter to count up and the tuned frequency to increase.

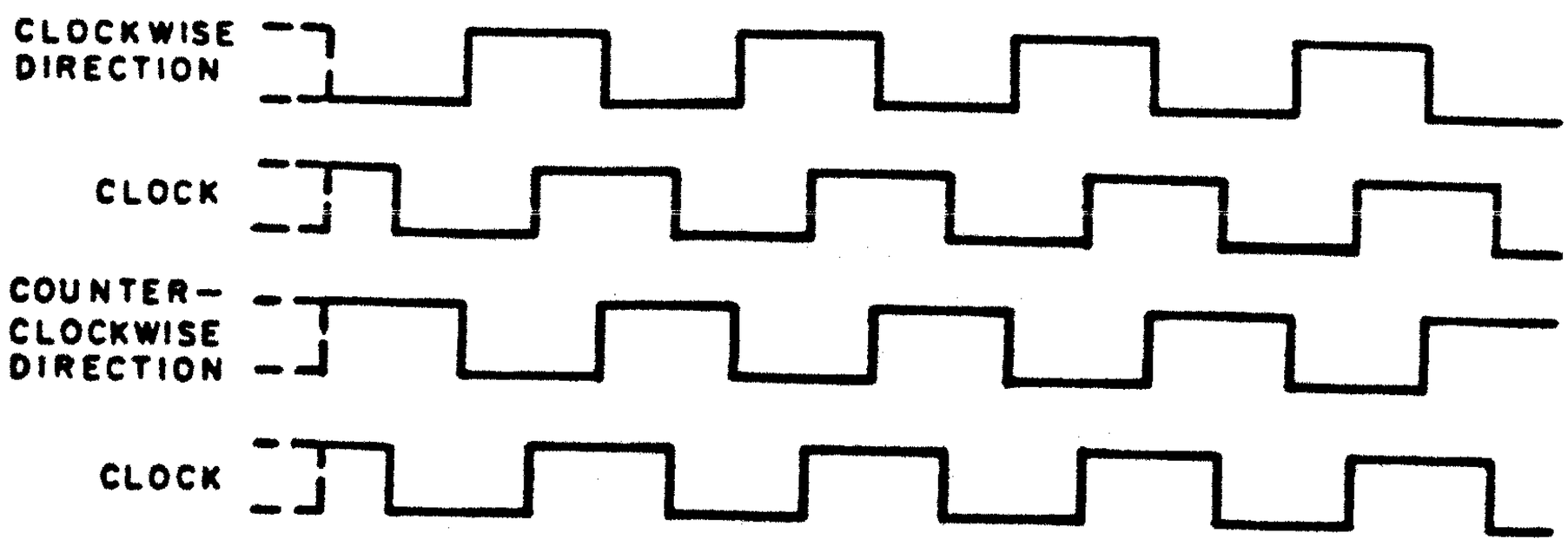


Figure 3-36. Encoder Assembly Timing Diagram

If the tuning knob is rotated counterclockwise, the sequence of outputs is reversed; the direction square wave lags the clock square wave. In this case the direction line will be low when the clock line swings high causing the counter to count down, thus reducing the tuned frequency.

The two outputs of the encoder go through approximately 120 cycles per revolution of its input shaft. This causes a tuning step for roughly each 3^{o} of knob rotation.

The encoder assembly uses infrared optics to accomplish its internal functions. It is not considered a repairable assembly.

3.4.26 TYPE 791578-1 FREQUENCY DISPLAY (A8)

The Frequency Display accepts the multiplexed information from the Manual Tuning Up/Down Counter via connector J2 and displays it on seven LEDs on the front panel. The schematic diagram for this circuit is shown in **Figure 6-23.**

U1 to U7 are the seven segment common-cathode LED displays. All segments of each display are connected in parallel to the corresponding outputs of U8, a BCD to seven-segment decoder/driver. U8 accepts a BCD word on its A, B, C and D inputs, converts it to a seven-segment equivalent, and places the information on its a to g outputs. The outputs are internally current-limited to provide about 50 mA so that external resistors are not needed. To turn a particular digit on, its common cathode input must be logic low. This selection is provided by U9, a binary to octal decoder. It accepts the Q0 to Q2 data on its A, B, and C inputs and places a high on the Q output with the equivalent binary value. U10 is an eight-section buffer inverter, capable of providing up to 500 mA of sink current.

Operation of the circuit is described below. The Up/Down Counter places digit display information into the A, B, and C inputs of U9. BCD information enters the A, B, C and D lines of U8. In U8, this information is decoded into a seven-segment number and sent to all the LEDs. U9 enables only one display at a time as commanded by its input information. Since the rate of change is 2 kHz, each digit is refreshed every 4 msec (2 kHz/8). This flicker rate is undetectable by the human eye.

Transistor Q1 is used for the intensity control. It is connected as a pass transistor from the unregulated 10 V to the supply voltage of U8. As the supply voltage of U8 is increased the current delivered to the LEDs will increase, giving more intensity. R1, R2, and R4 are a voltage divider which bounds the emitter voltage of Q1 between about 4.5 V and 7 V.

The decimal point, CR1, is always on, receiving its current from Q1 through resistor R3.

3.4.27 TYPE 791827 BFO SWITCH (A9)

The BFO Switch schematic diagram is **Figure 6-25.** Three thumbwheel switches provide a BFO variation of ±8.9 kHz from 455 kHz. The +, 0, -, thumbwheel provides the direction of offset, the second thumbwheel varies in range from 0 to 8, and the third thumbwheel varies in range from 0 to 9. A '0' setting of the direction thumbwheel causes the BFO to return automatically to 455 kHz (regardless of the other thumbwheel settings). The truth table for these switches is given in **Table 3-9.**

Table 3-9. BFO Switch Truth Tables

NUMERIC	OUTPUT				SIGN	OUTPUT
DIGIT	2^3	2^2	2^1	2^0	DIGIT	+ 0 -
0	X	X	X	X	+	X O O
1	X	X	X	O	O	X X O
2	X	X	O	X	-	O O X
3	X	X	O	O		
4	X	O	X	X		
5	X	O	X	O		
6	X	O	O	X		
7	X	O	O	O		
8	O	X	X	X		
9	O	X	X	O		

X denotes shorted to common
O denotes open

3.4.28 TYPE 796053 FRONT PANEL CONTROL (A10)

The Front Panel Control consists of the Upper and Lower Panel Control boards joined by a 40-pin ribbon connector. This connector is attached to the Front Panel Interconnect (A6A2) and controls the manual selection of detection mode, gain mode, meter mode, IF bandwidth, RF gain, and headphone levels. Signals for the phone outputs also connect to the lower panel control through the Front Panel Interconnect. The functions of the IF bandwidth and detection mode switches are described in **paragraph 3.3.3.9** and **3.3.3.10.**

3.4.29 TYPE 791583 UPPER PANEL CONTROL (A10A1)

The Upper Panel Control allows selection of detection mode, gain mode, and meter mode. Each gang of switches mechanically operates to allow only one pushbutton to be depressed at any time. All control lines connect to the Front Panel Interconnect card. The schematic diagram for this circuit is shown in **Figure 6-25.**

3.4.30 TYPE 796054 LOWER PANEL CONTROL (A10A2)

The Lower Panel Control allows selection of IF bandwidth and variation of RF GAIN and PHONE LEVEL potentiometers. The schematic for this circuit is **Figure 6-25.** This card also contains the amplifiers to drive the headphone outputs. A simplified schematic of the headphone audio routing is shown in **Figure 3-37.** This circuit provides two new switches at the receiver front panel, designated ISB AUDIO "LSB" and ISB AUDIO "USB". When the receiver is operating in Independent Sideband mode (ISB), the upper sideband audio is applied to terminal E3 of A10A2, and the lower sideband audio is supplied to terminal E9. Switches S2A and S2B (ISB AUDIO) are interlocked such that only one may be depressed at a time. The switches are wired to supply the selected sideband audio to one end of both ganged potentiometers, R2A and R2B. The signal is then fed from the wiper of each potentiometer to the associated audio amplifier, U1A or U1B. Therefore, the selected sideband audio signal will be heard in both channels of a stereo headphone connected to the front panel phone jack, J13.

NOTE: The demodulated audio signals are always supplied to terminals E3 and E9 of the Lower Panel Control board, type 796054, for application to the headphone amplifiers, U1A and U1B. Refer to **Figure 3-37.** In all detection modes except ISB, the same audio signal line (COMBINED AUDIO) is connected to both terminals. When the ISB detection mode pushbutton (A10A1S3D) is depressed, the audio signal routing is changed. Terminal E3 is still connected to the COMBINED AUDIO line, but terminal E9 is now connected to the ISB/LSB AUDIO line. In this mode, terminal E3 receives the USB audio, and terminal E9 receives the LSB audio. The ISB AUDIO pushbuttons allow the operator to select either sideband signal to drive both headphone amplifiers. However, with a remote-control option installed, it is possible to remotely select a different detection mode (AM, FM, etc.) while the ISB detection mode pushbutton is depressed. In this case, the remotely selected detection mode audio will only appear on the COMBINED AUDIO line connected to E3. If neither ISB AUDIO pushbutton is depressed, the remotely selected detection mode audio will drive headphone amplifier U1A, but no LSB signal is supplied to U1B because the ISB Detector/Audio module is not switched on. If the ISB AUDIO pushbutton "USB" is depressed, both amplifiers are driven from COMBINED AUDIO, and the remotely selected detection mode audio will be heard in both phones. However, if the ISB AUDIO pushbutton "LSB" is depressed, both amplifiers are connected to the "dead" ISB/LSB AUDIO line, and no audio will be heard. Therefore, both ISB AUDIO pushbuttons should be left in the "OUT" (non-selected) position unless the receiver is being manually operated in the ISB detection mode. Also note that when the ISB detection mode is remotely selected, the lower sideband audio signal will not be supplied to the ISB AUDIO headphone circuit unless the ISB detection mode is manually selected.

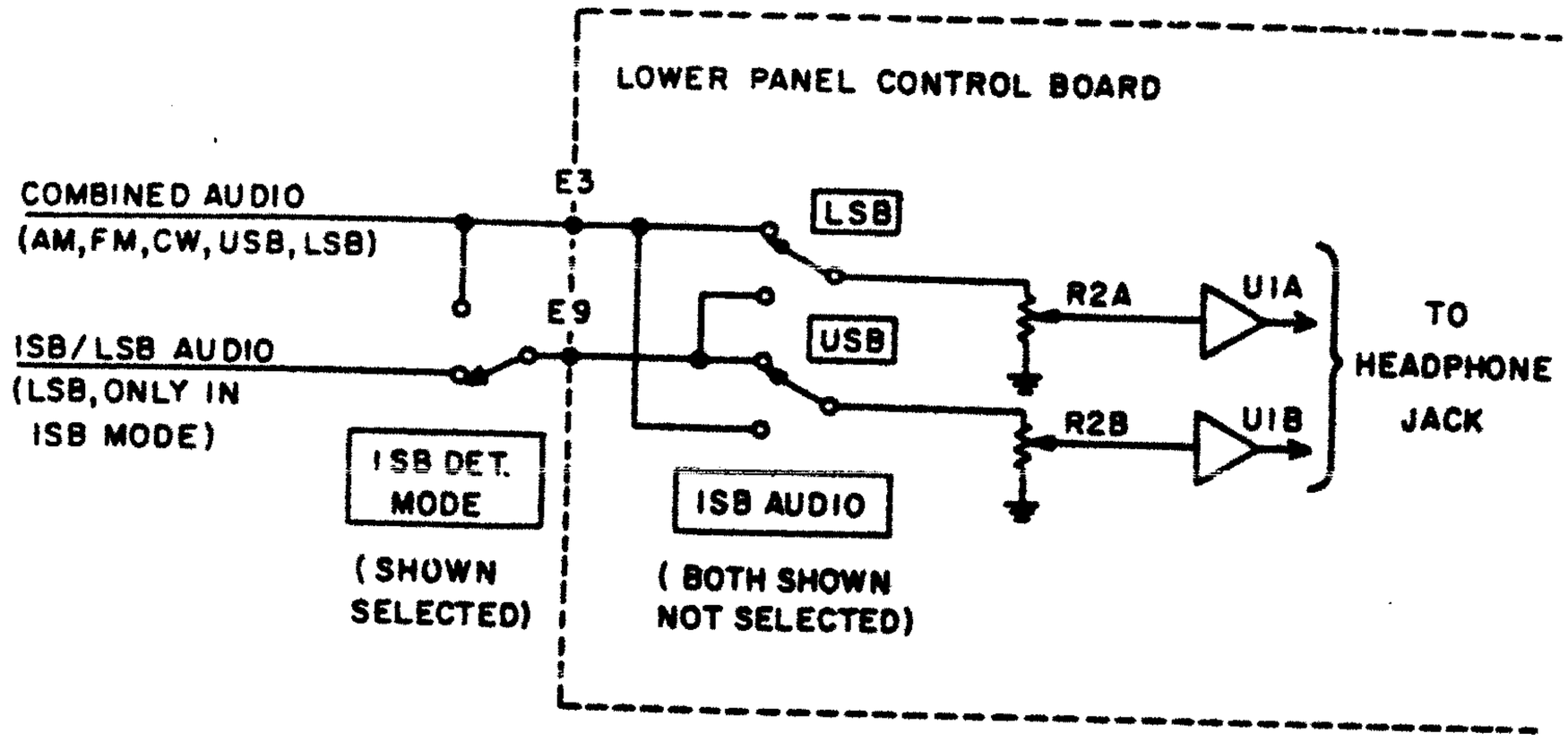


Figure 3-37. Simplified Headphone Audio Routing.

3.4.31 TYPE 791826 LOWER PANEL CONTROL (A10A2)

The Lower Panel Control allows selection of IF bandwidth and variation of RF gain and phone level potentiometers. The schematic diagram for this circuit is **Figure 6-20.** This card also contains the amplifiers to drive the headphone outputs. The amplifiers operate independently. They receive the same signal in all detection modes except ISB. In this mode, amplifier U1A receives the upper sideband information while U1B receives the lower sideband information. No damage will be done to the amplifiers when using mono headphones; however, LSB in the ISB mode will not be monitored.

3.4.32 MAIN CHASSIS REGULATOR, U4 (WJ-8718A/8718-9 only)

Main chassis IC voltage regulator U4 supplies +12 V to the line audio amplifier circuit on Type 746001 Audio Amplifier (A4A10). Regulator U4 is rated at 1 A, and will automatically shut down if the current exceeds that value.

3.4.33 MAIN CHASSIS BATTERY, BT1

Battery BT1 is a rear panel mounted 2.5 Volt nickel-cadmium battery connected to the Main Tuning Up/Down Counter, A6A1. When AC power is deenergized, BT1 keeps the A6A1 frequency memory alive, so that the receiver remembers the frequency it was tuned to prior to power interruption.